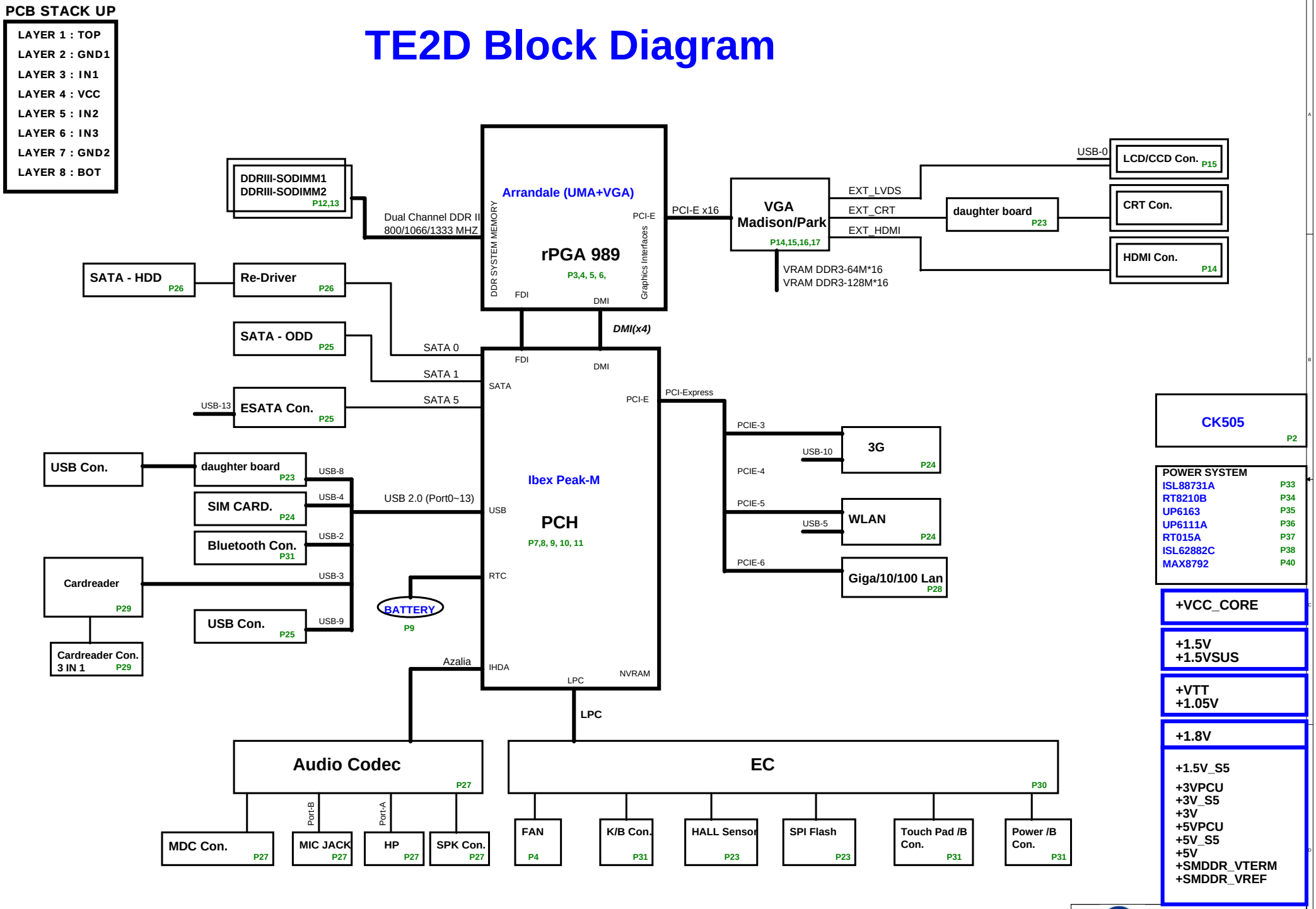
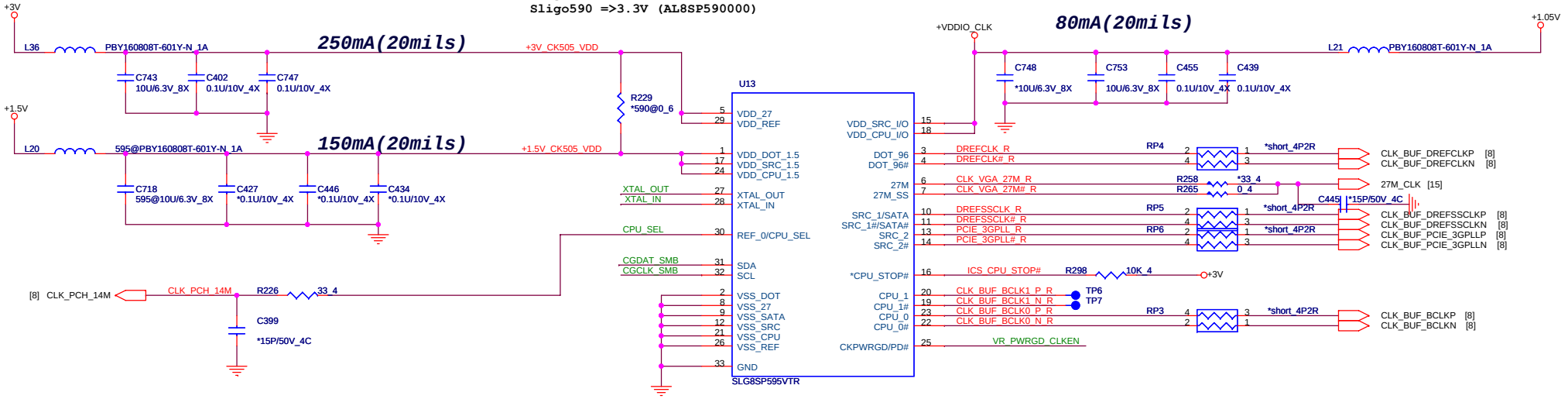
TE2D Block Diagram

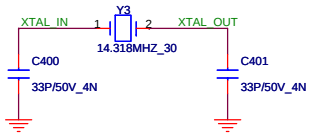


CLOCK Gen [CLK]

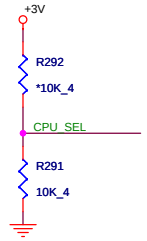
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

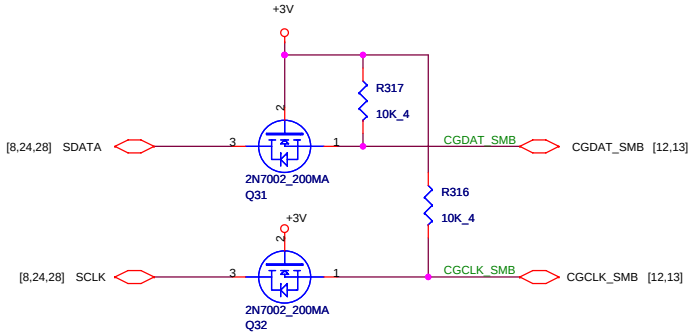


CLK CPU_SEL



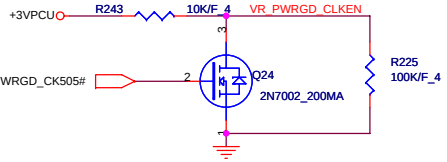
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

Change to +3VPCU
(follow CRB)

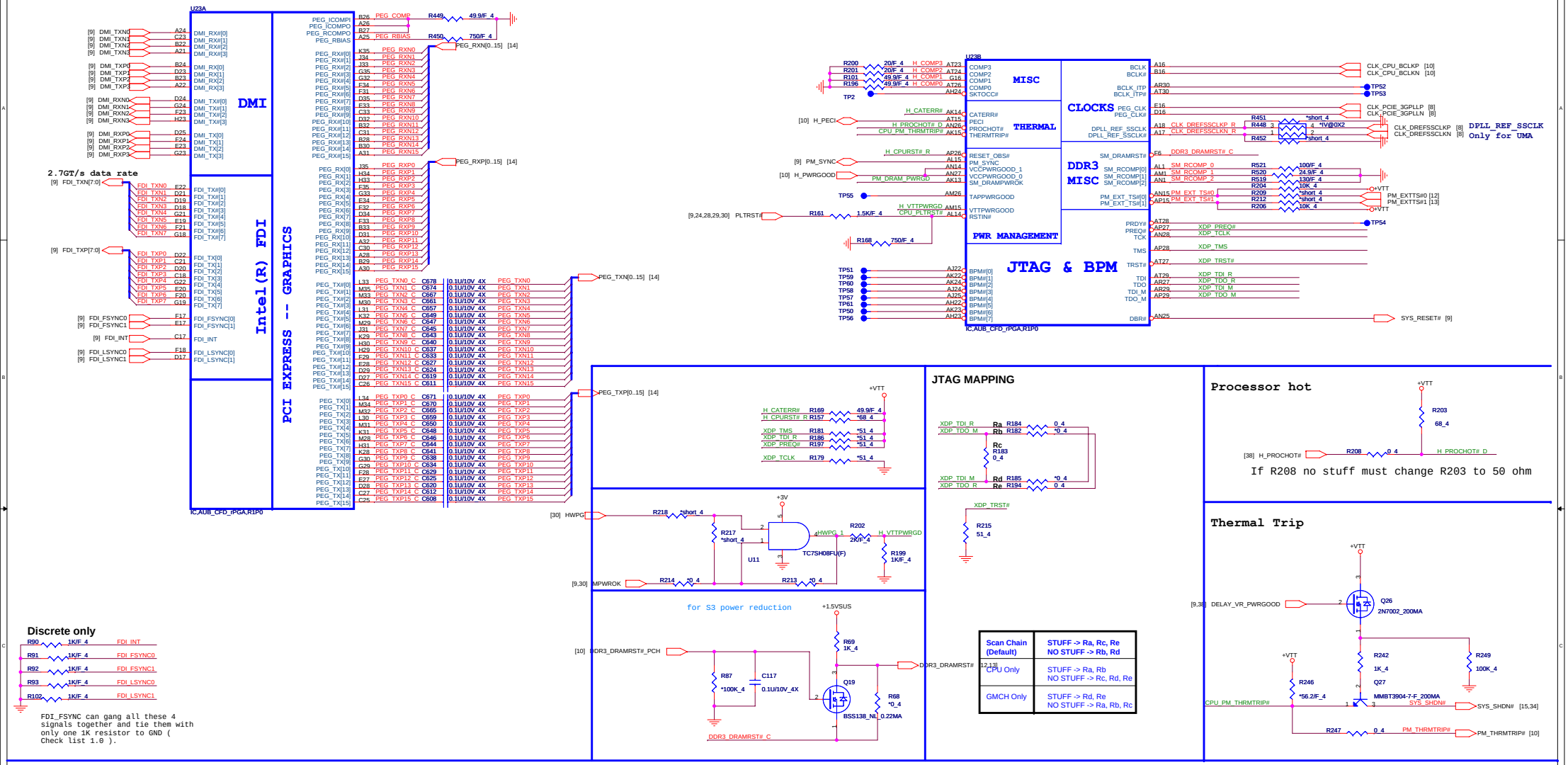


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	CLOCK GENERATOR	2A

Date: Friday, March 19, 2010 Sheet 2 of 45



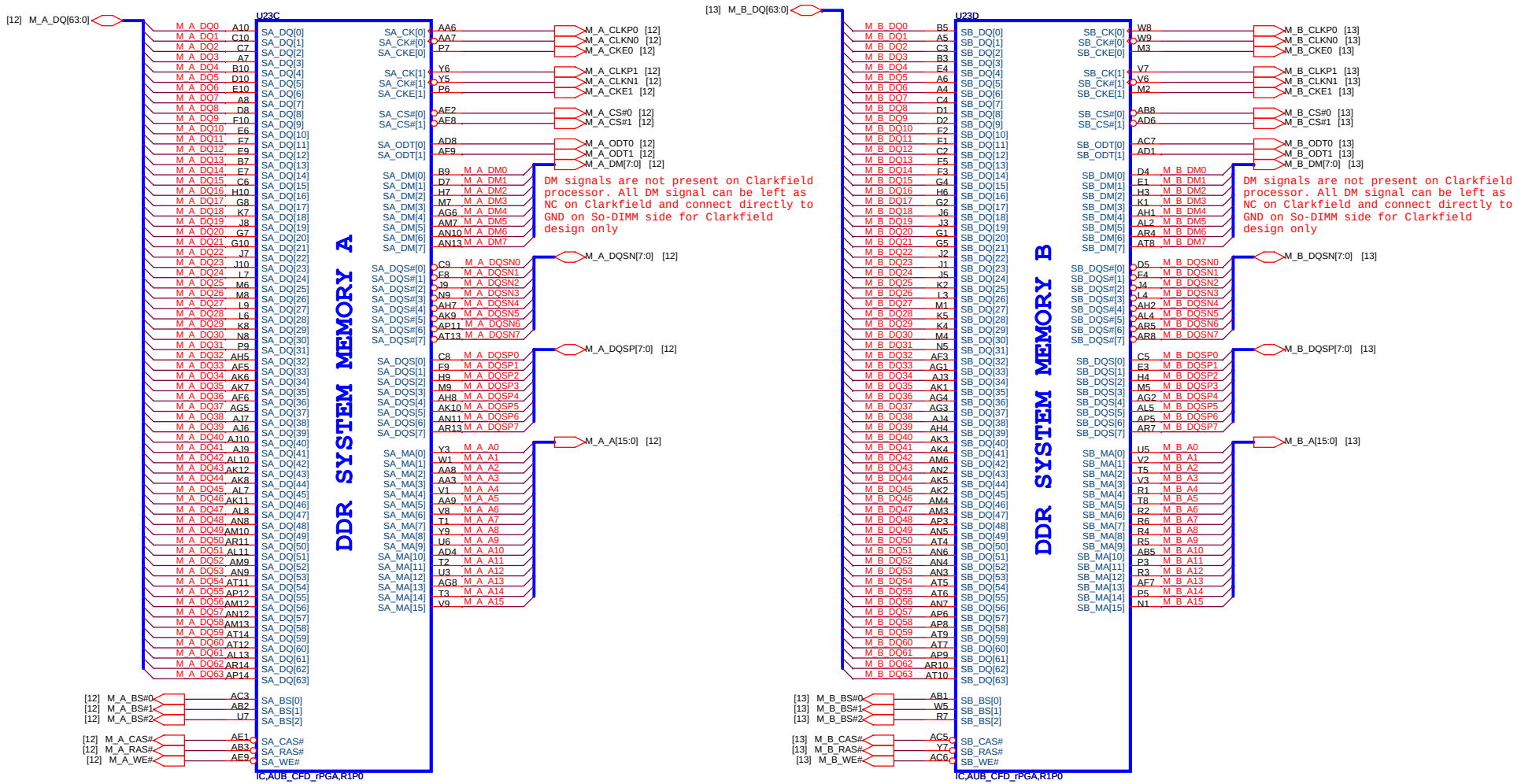
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	2A
Date: Tuesday, March 09, 2010	Sheet 3 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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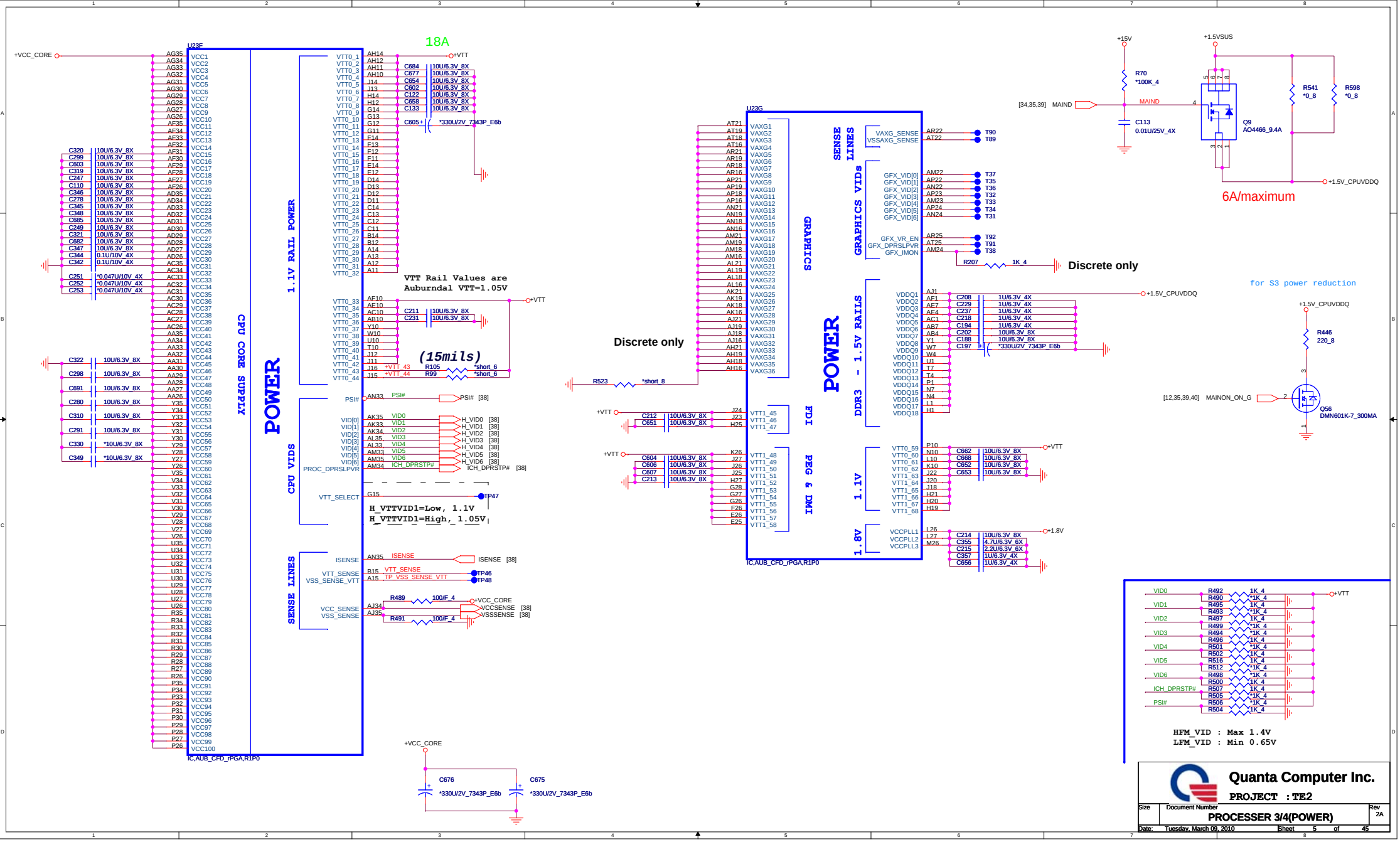
PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	2A

Date: Thursday, February 25, 2010 Sheet 4 of 45


18A
U23F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
IC,AUB_CFD_rPGA,R1P0
+VCC_CORE
+VTT
VTT Rail Values are
Auburndal VTT=1.05V
(15mils)
Discrete only
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
U23G
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
FDI
PEG & DMI
1.1V
1.8V
IC,AUB_CFD_rPGA,R1P0
+15V
+1.5VSUS
MAIND
Q9
AO4466_9.4A
+1.5V_CPUVDDQ
6A/maximum
Discrete only
for S3 power reduction
+1.5V_CPUVDDQ
Q56
DMN601K-7_300MA
MAINON_ON_G
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : TE2
PROCESSER 3/4(POWER)
Size
Document Number
Rev
2A
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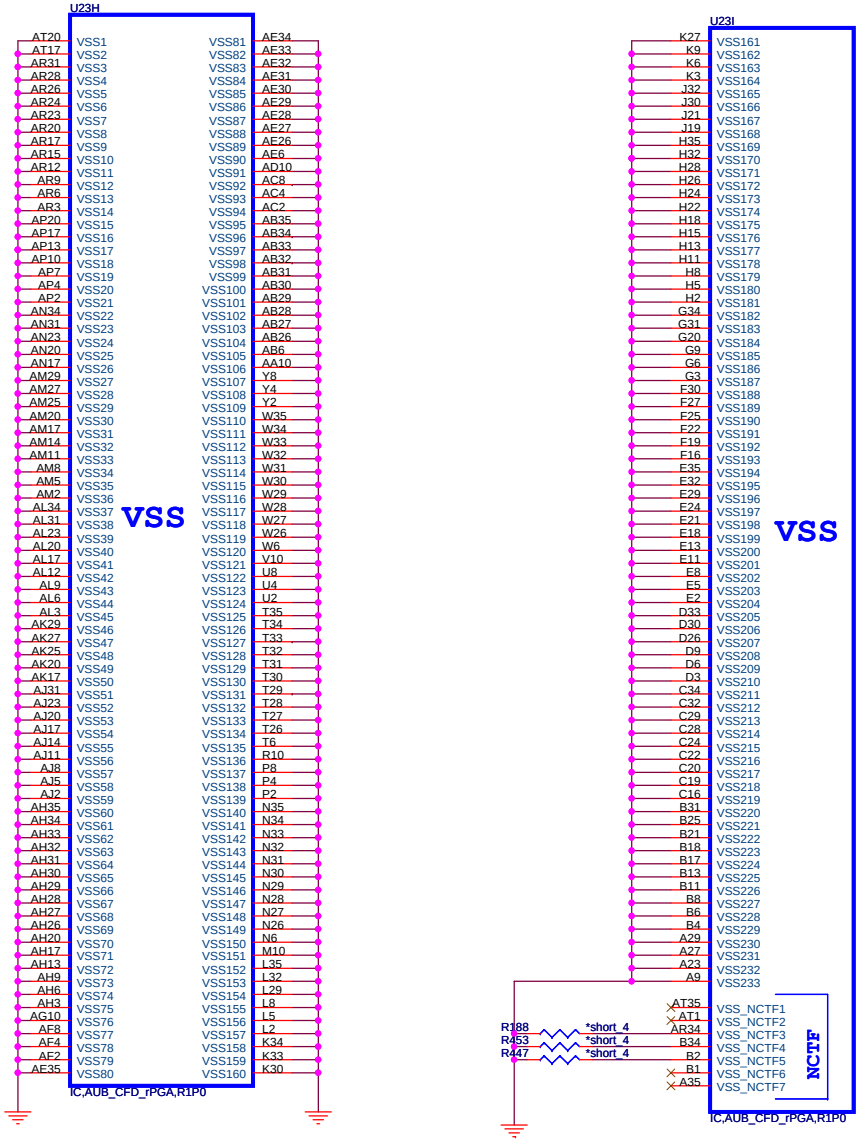
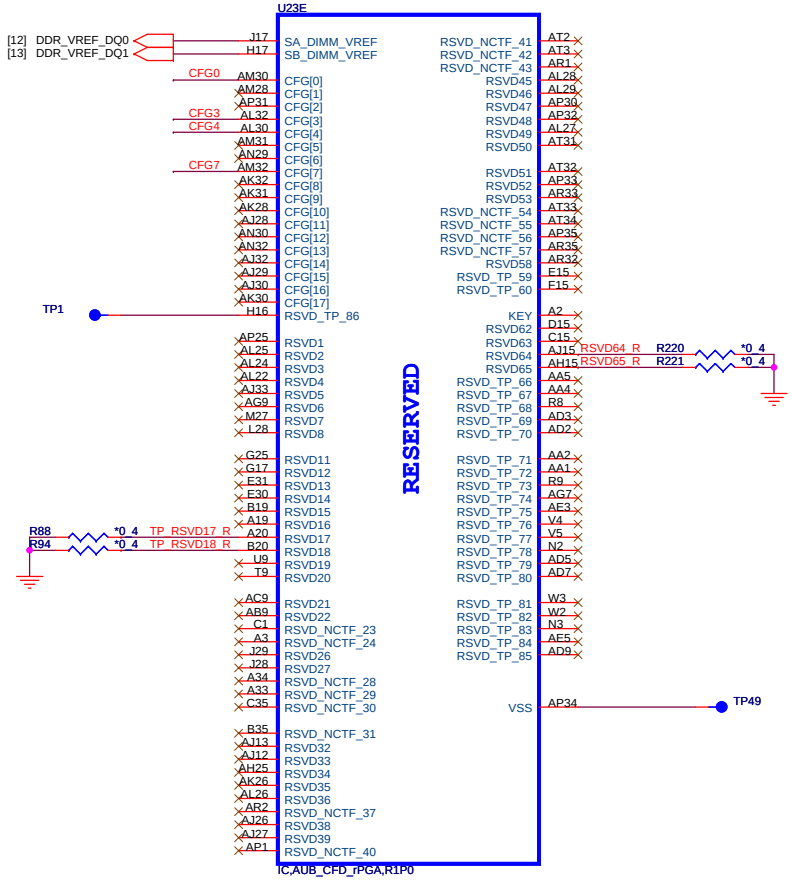
Sheet 5 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

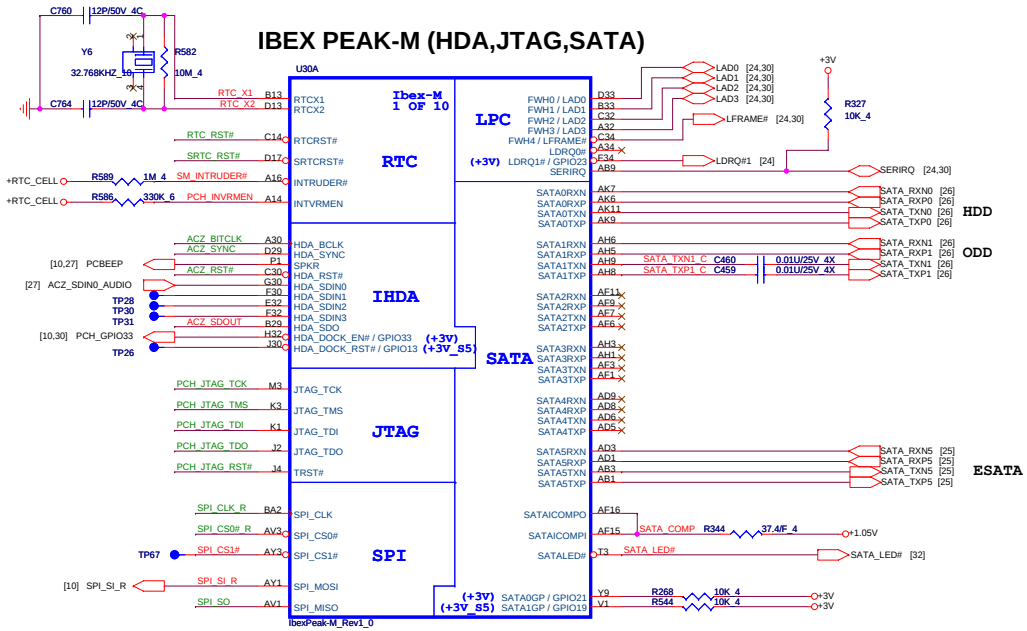
Quanta Computer Inc.

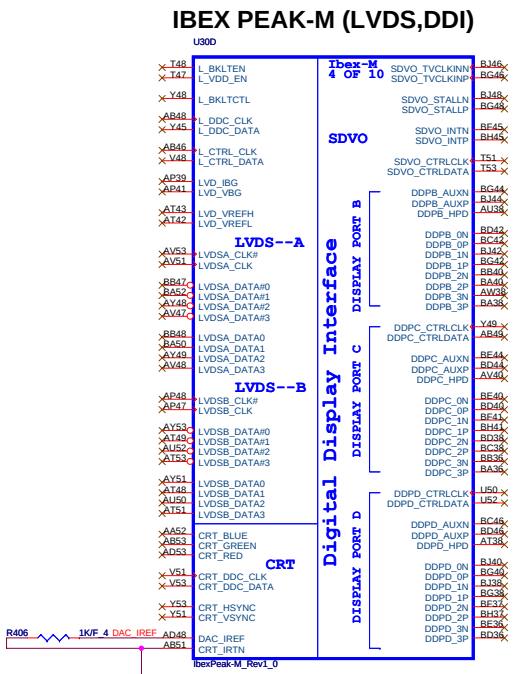
PROJECT : TE2

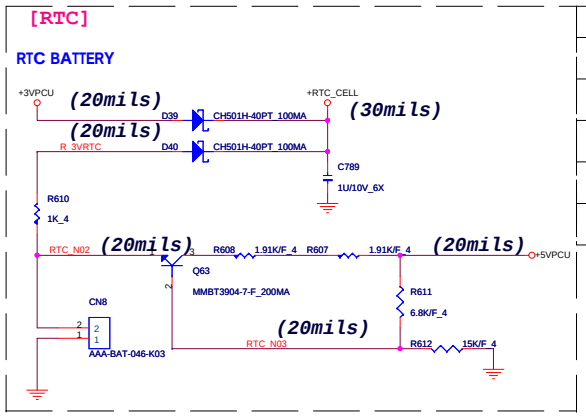
Size	Document Number	Rev
	PROCESSER 4/4 (GND)	2A

Date: Tuesday, March 09, 2010 Sheet 6 of 45

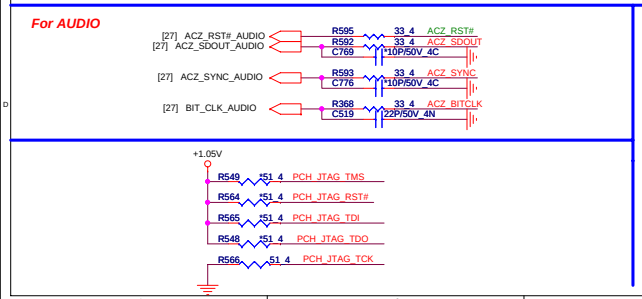
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

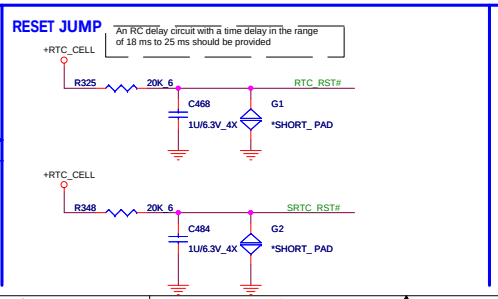


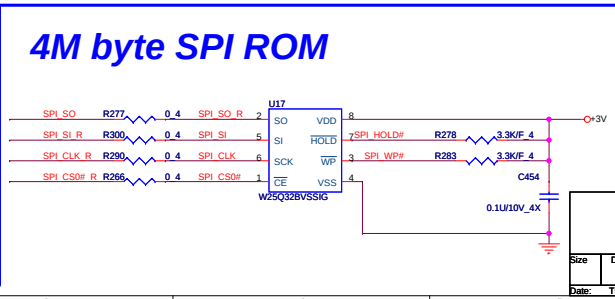




Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC







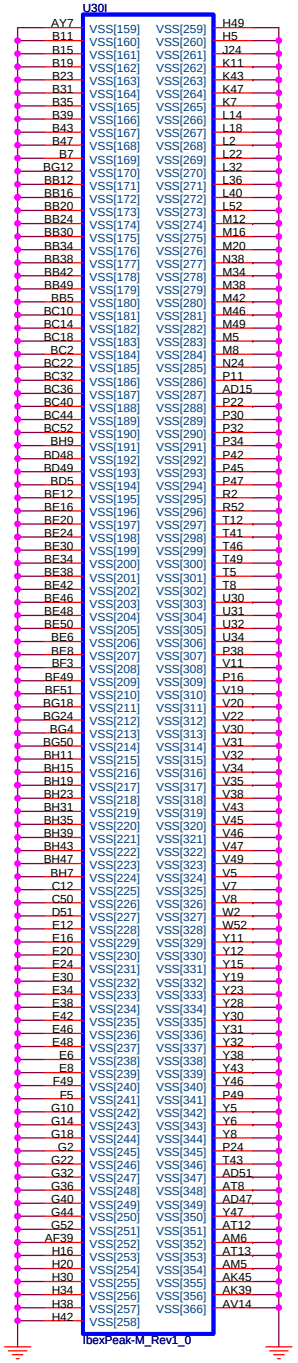
PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : TE2

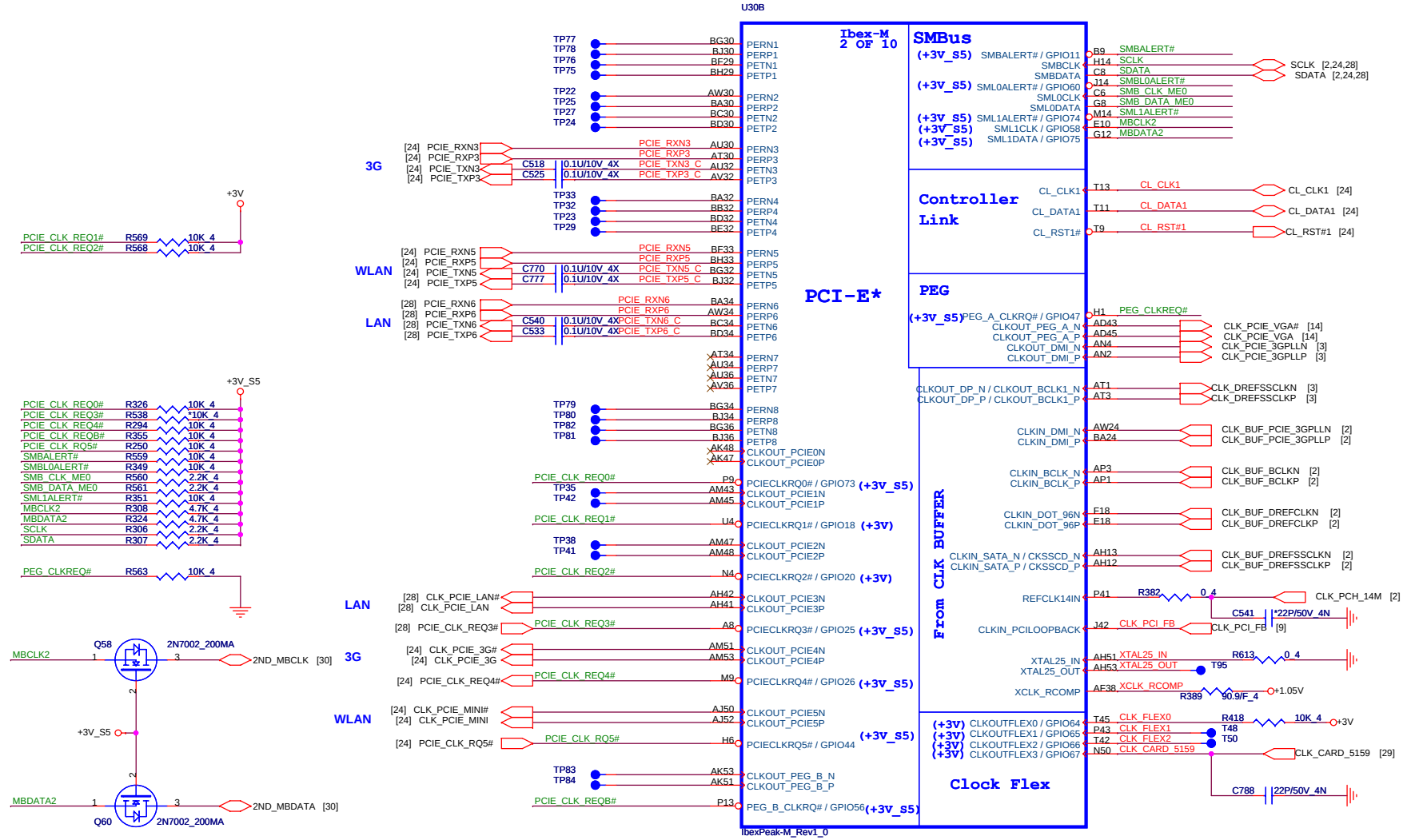
Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	2A

Date: Tuesday, March 09, 2010 Sheet 7 of 45

IBEX PEAK-M (GND)

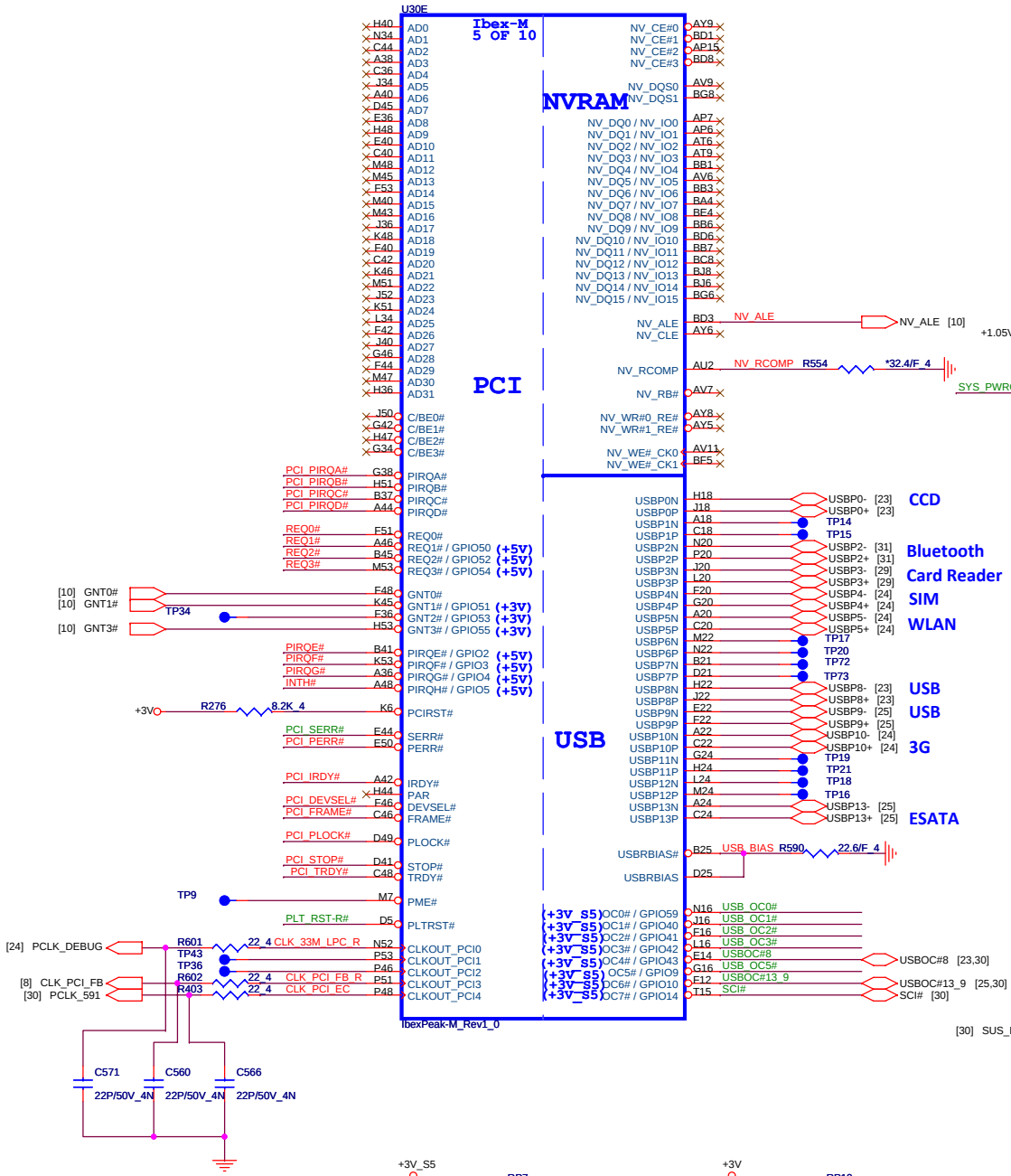


IBEX PEAK-M (PCI-E,SMBUS,CLK)

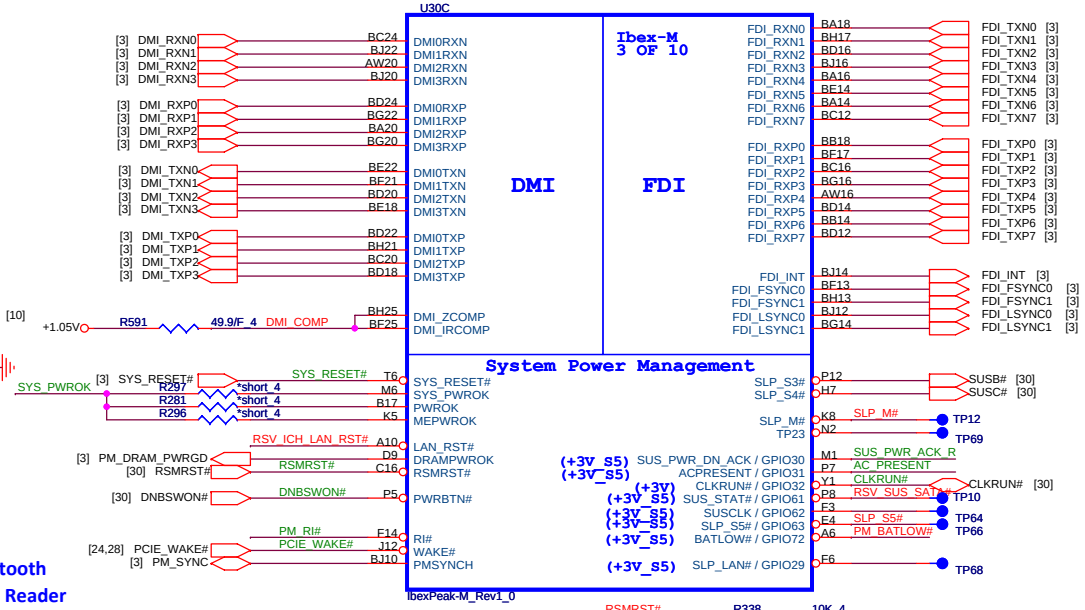


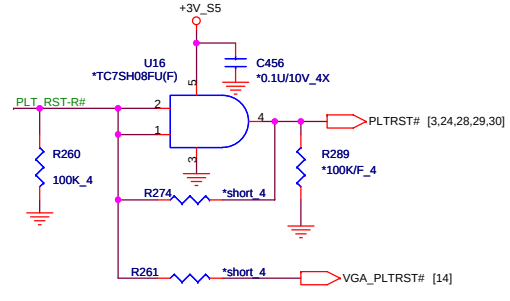
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev 2A
Date: Tuesday, March 09, 2010	Sheet 8 of 45	

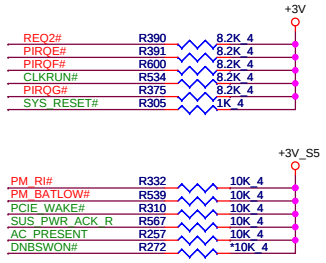
IBEX PEAK-M (PCI,USB,NVRAM)

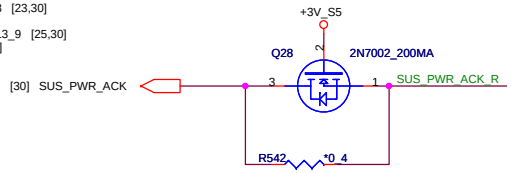


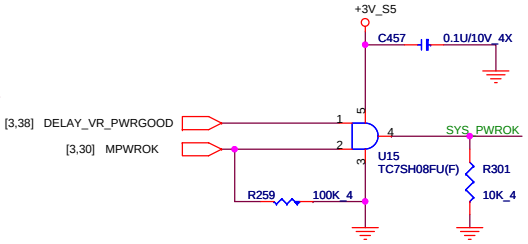
IBEX PEAK-M (DMI,FDI,GPIO)

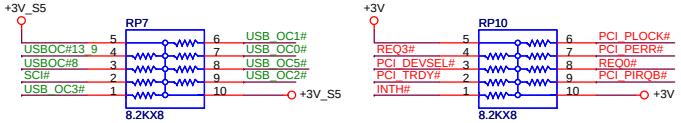












Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	2A

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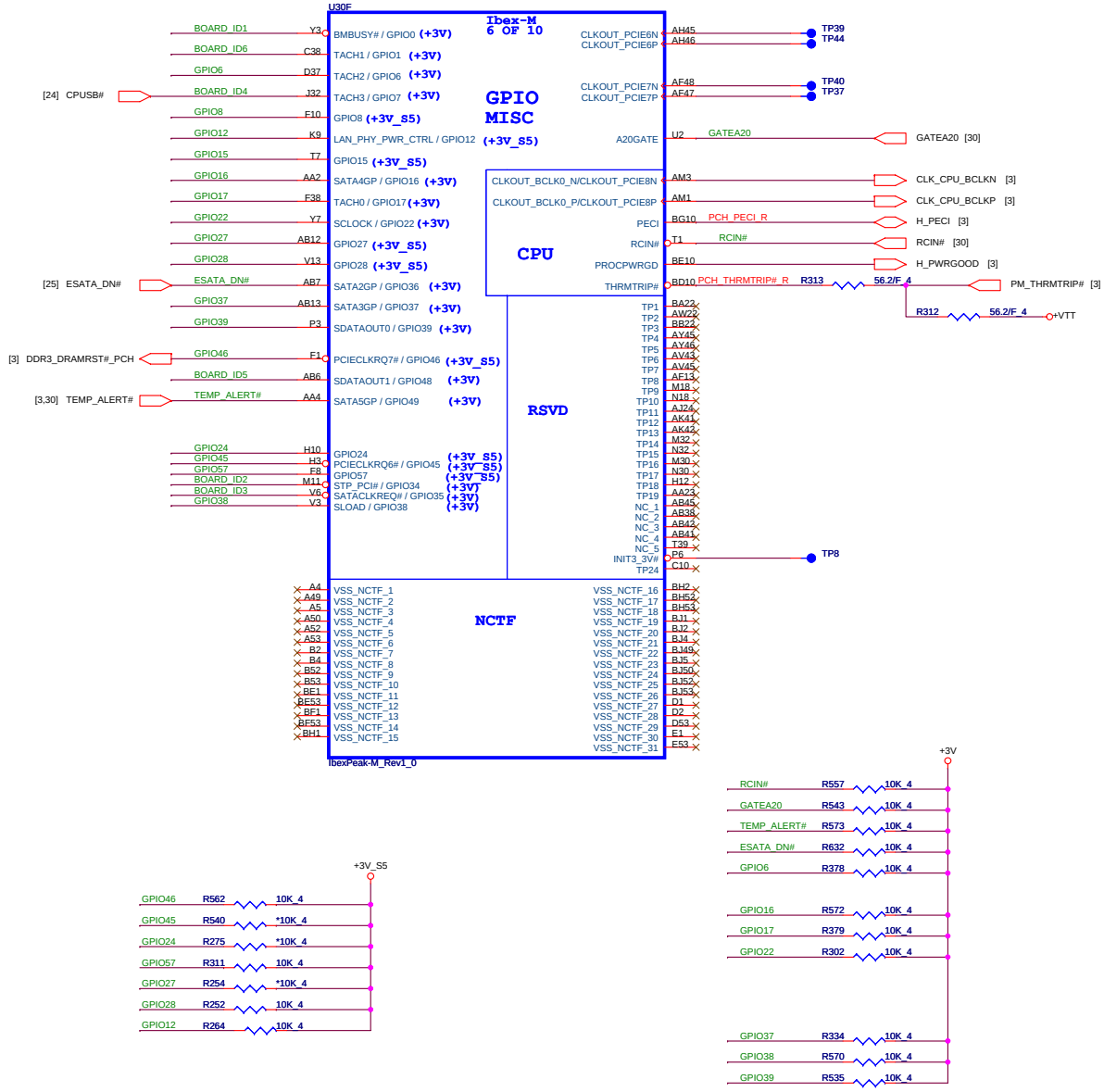
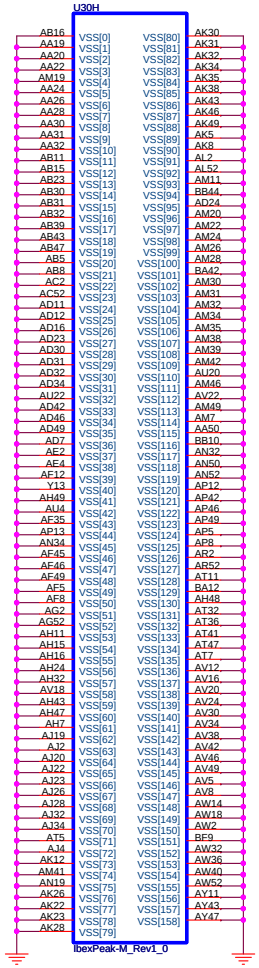
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

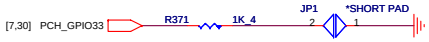
SPKR

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33



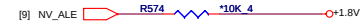
0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

NV_ALE



1 = Enabled
0 = Disabled (Default)

GPIO8

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

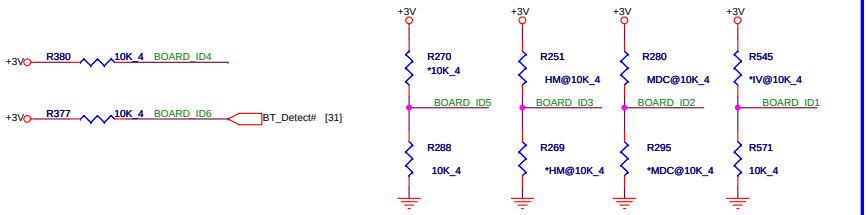
0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
W/ MDC W/O MDC		H L				
W/ HDMI W/O HDMI			H L			
W/O 3G W/ 3G				H L		
15" 14"					H L	
W/O BT W/ BT						H L

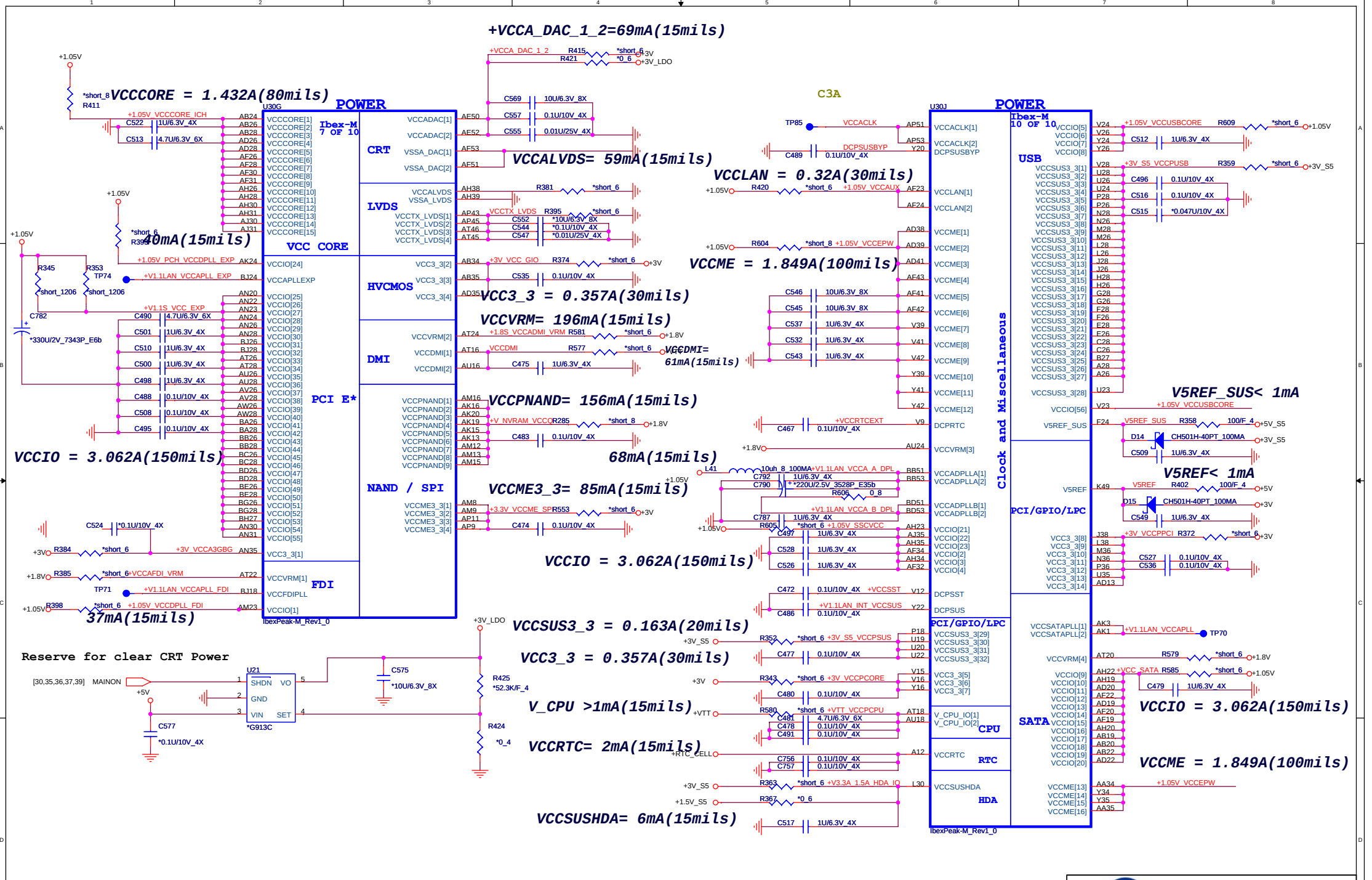


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	2A

Date: Friday, March 19, 2010 Sheet 10 of 45



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PROJECT : TE2

Size	Document Number	Rev
	PCH 5/5 (POWER)	2A

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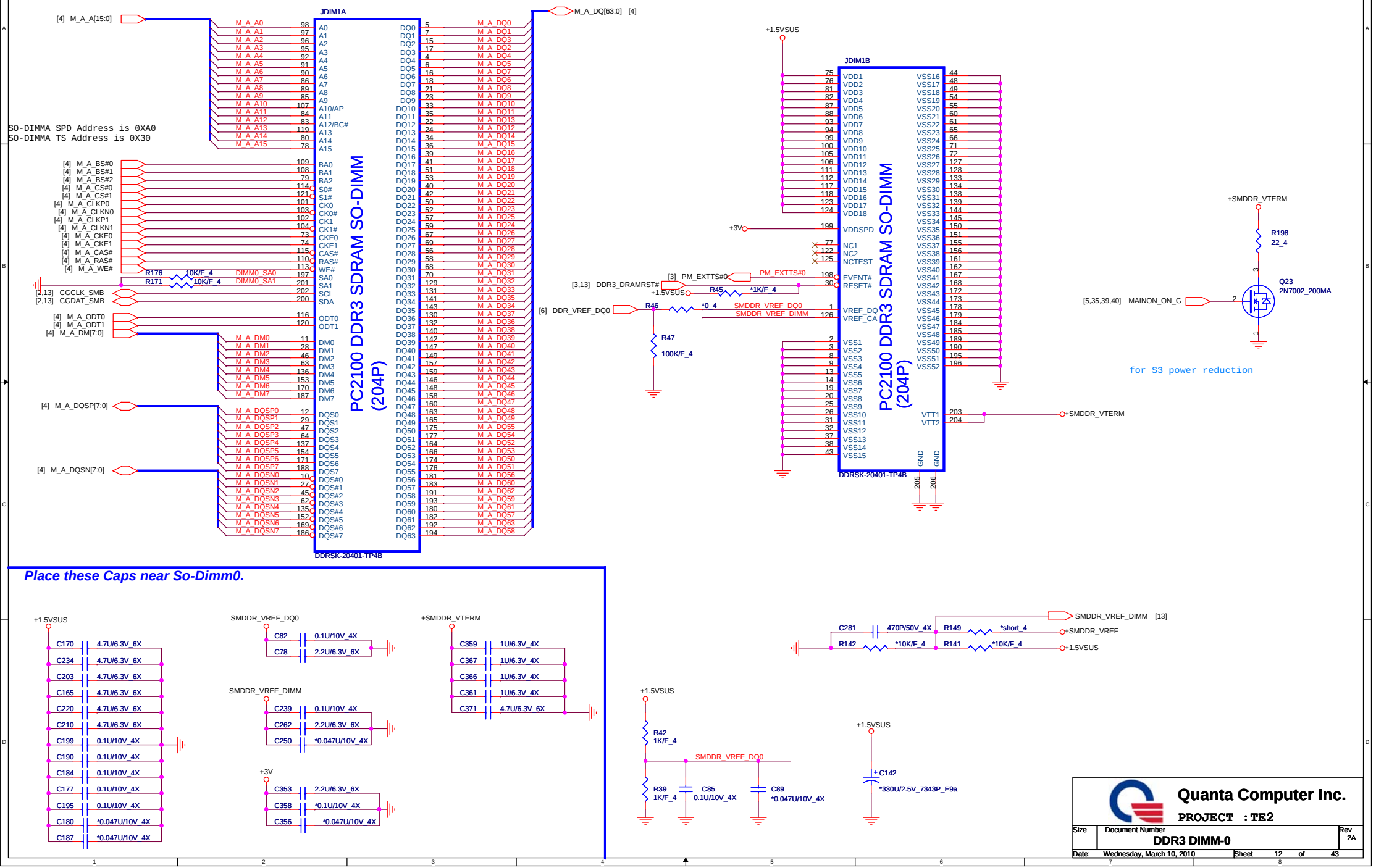

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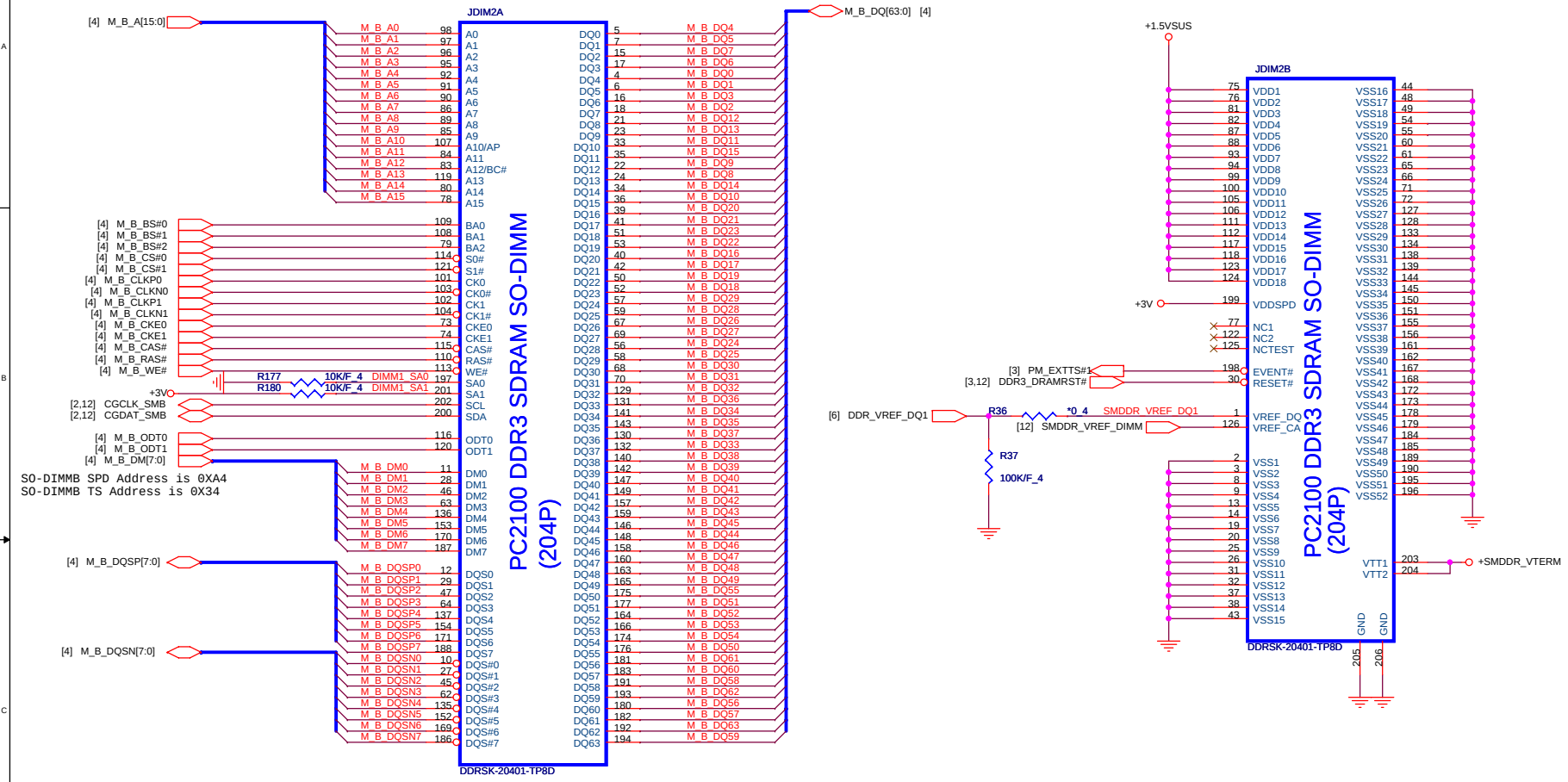
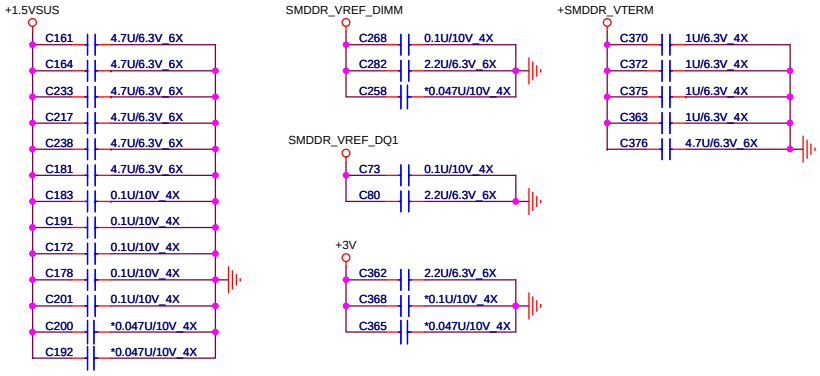
PROJECT : TE2

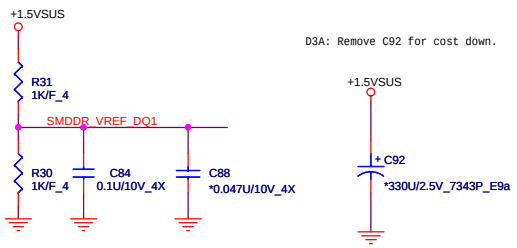
Size	Document Number	Rev
	DDR3 DIMM-0	2A

Date: Wednesday, March 10, 2010 Sheet 12 of 43



Place these Caps near So-Dimm1.



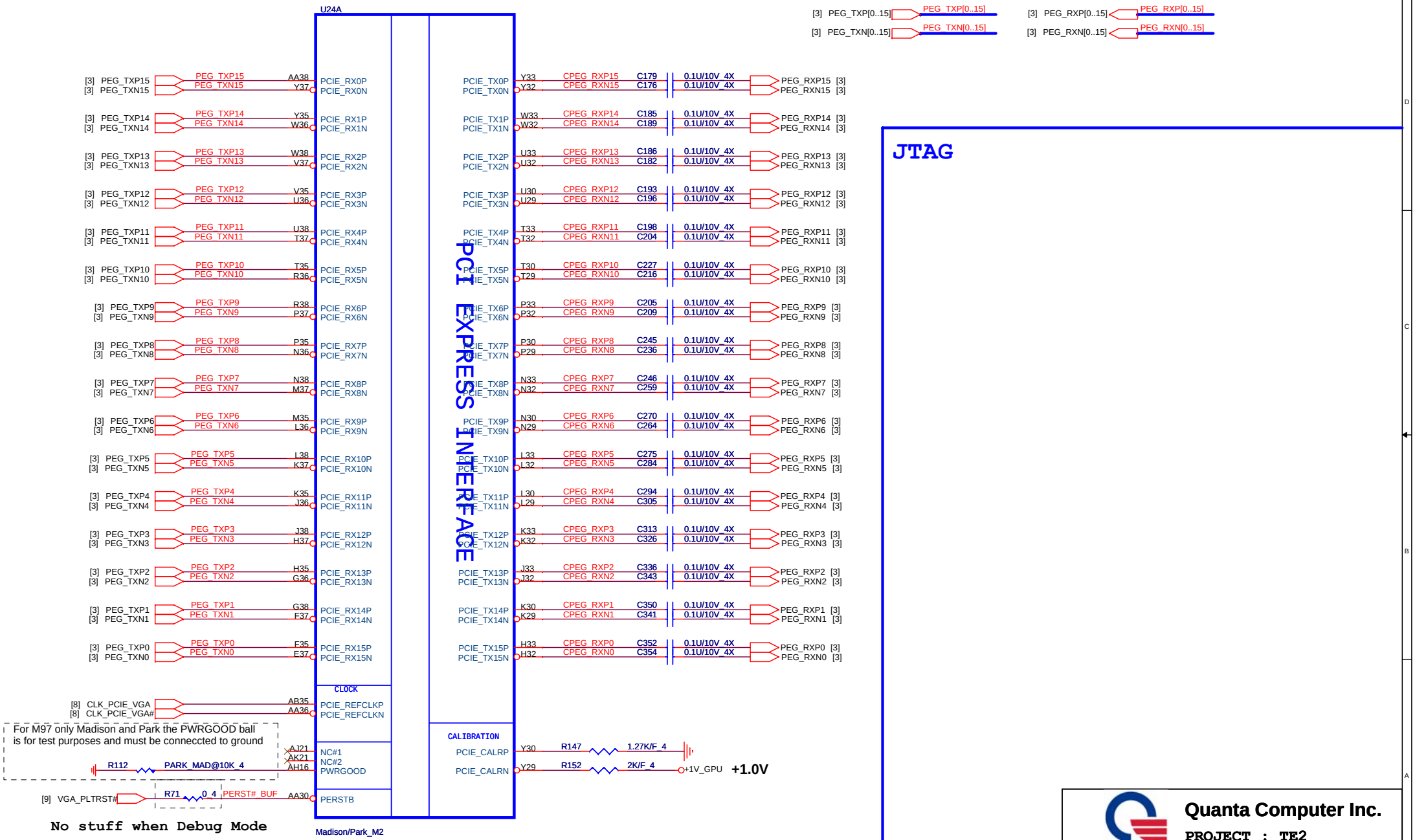


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	DDR3 DIMM-1	2A

Date: Wednesday, March 10, 2010 Sheet 13 of 43



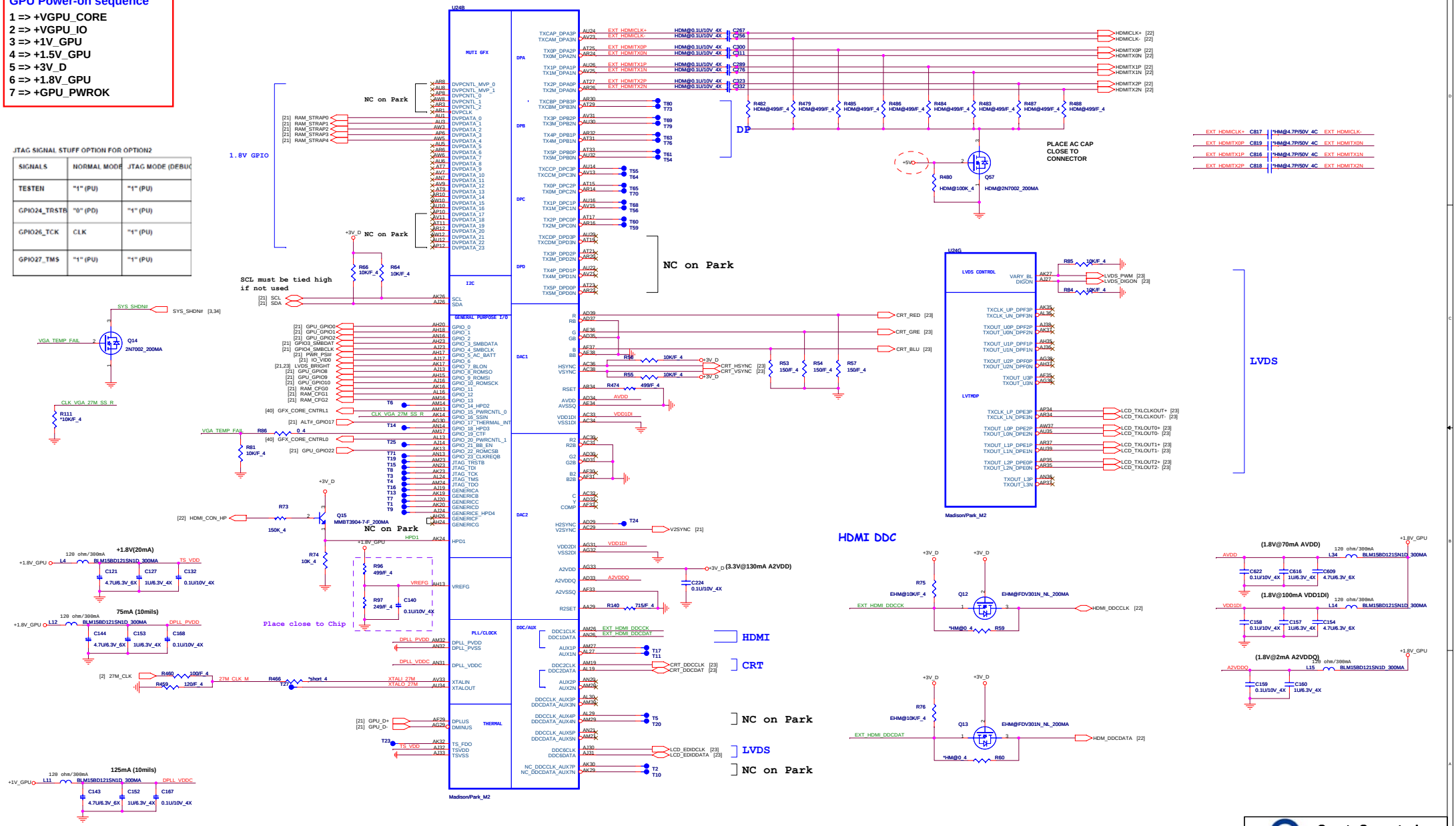
For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

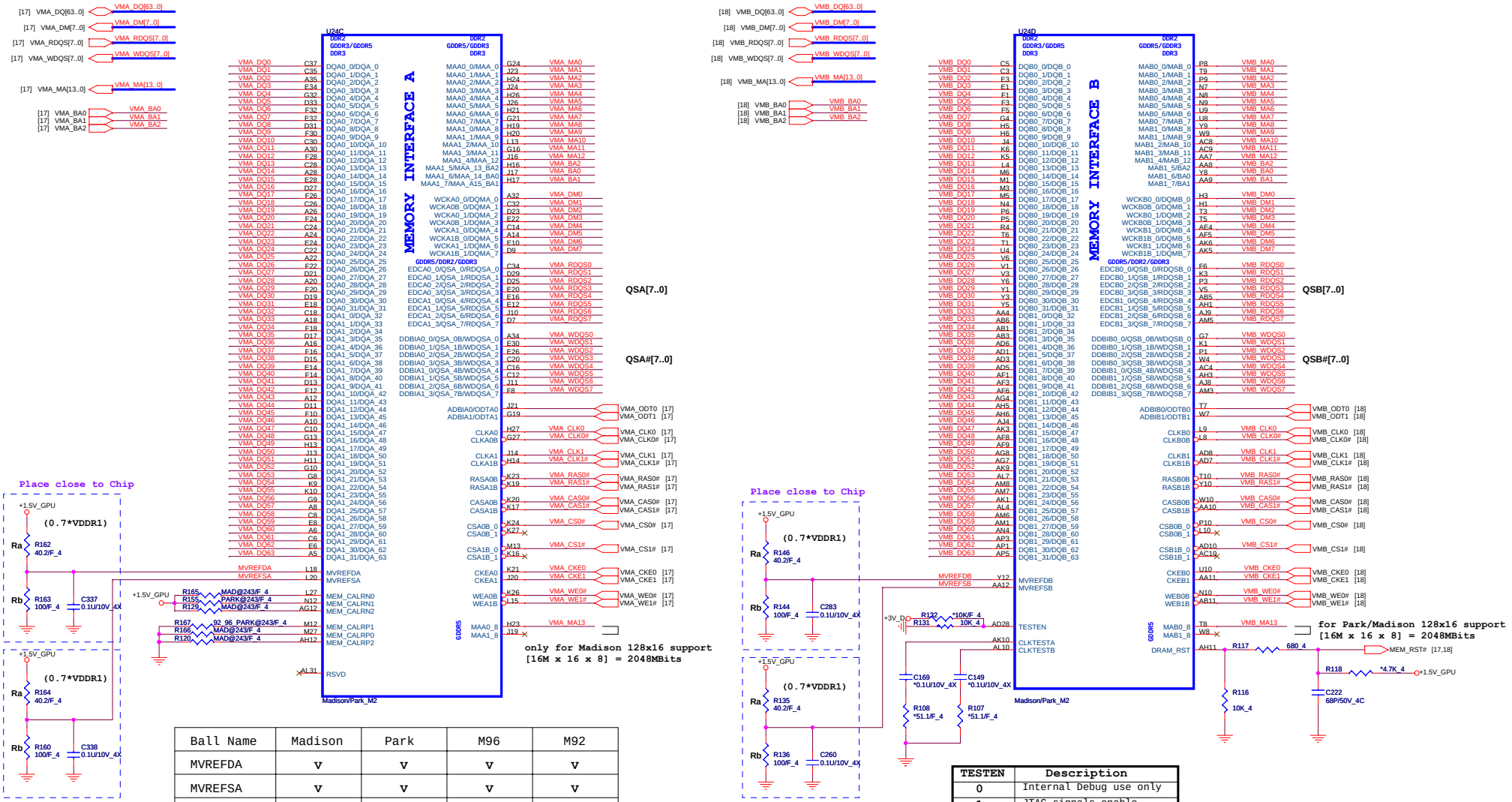
GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V_GPU
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => +GPU_PWROK

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)





Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

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PROJECT : TE2

Size	Document Number	Rev
	Madison/Park-MEM I/F	2A

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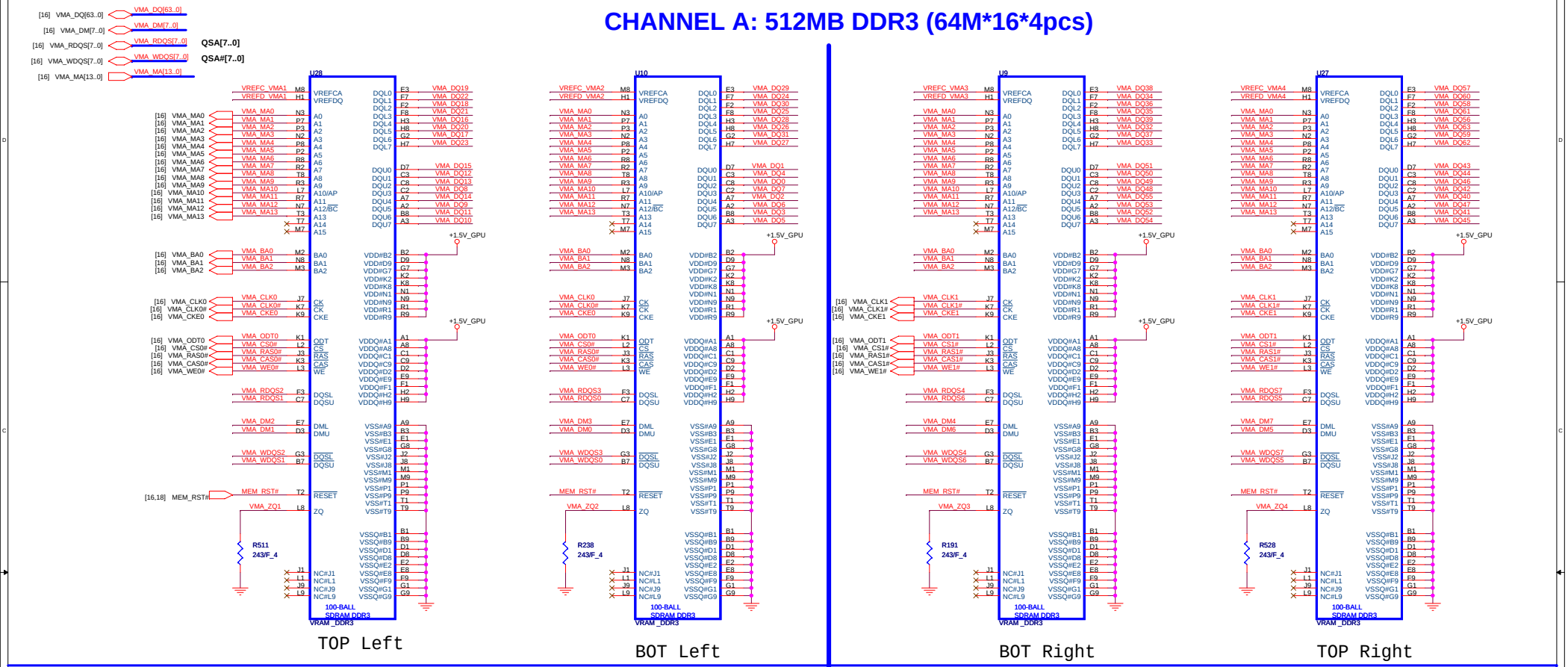
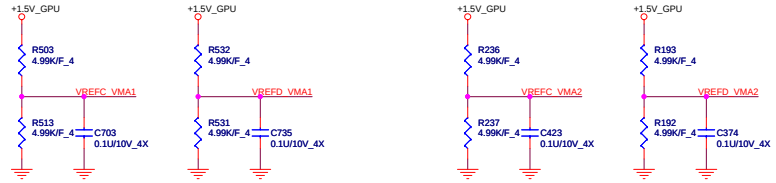
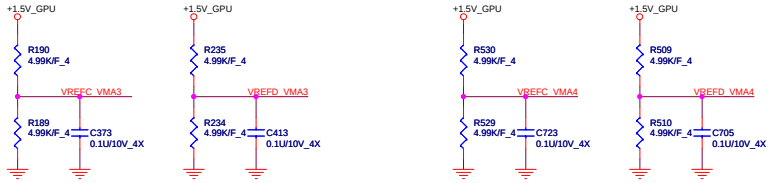
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



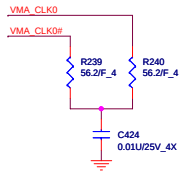
Group-A0 VREF



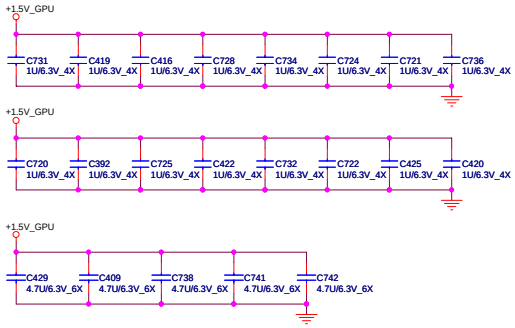
Group-A1 VREF



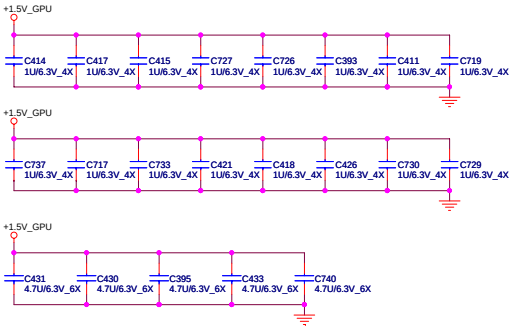
MEM_A0 CLK



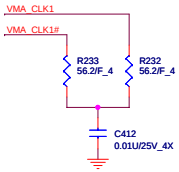
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	2A

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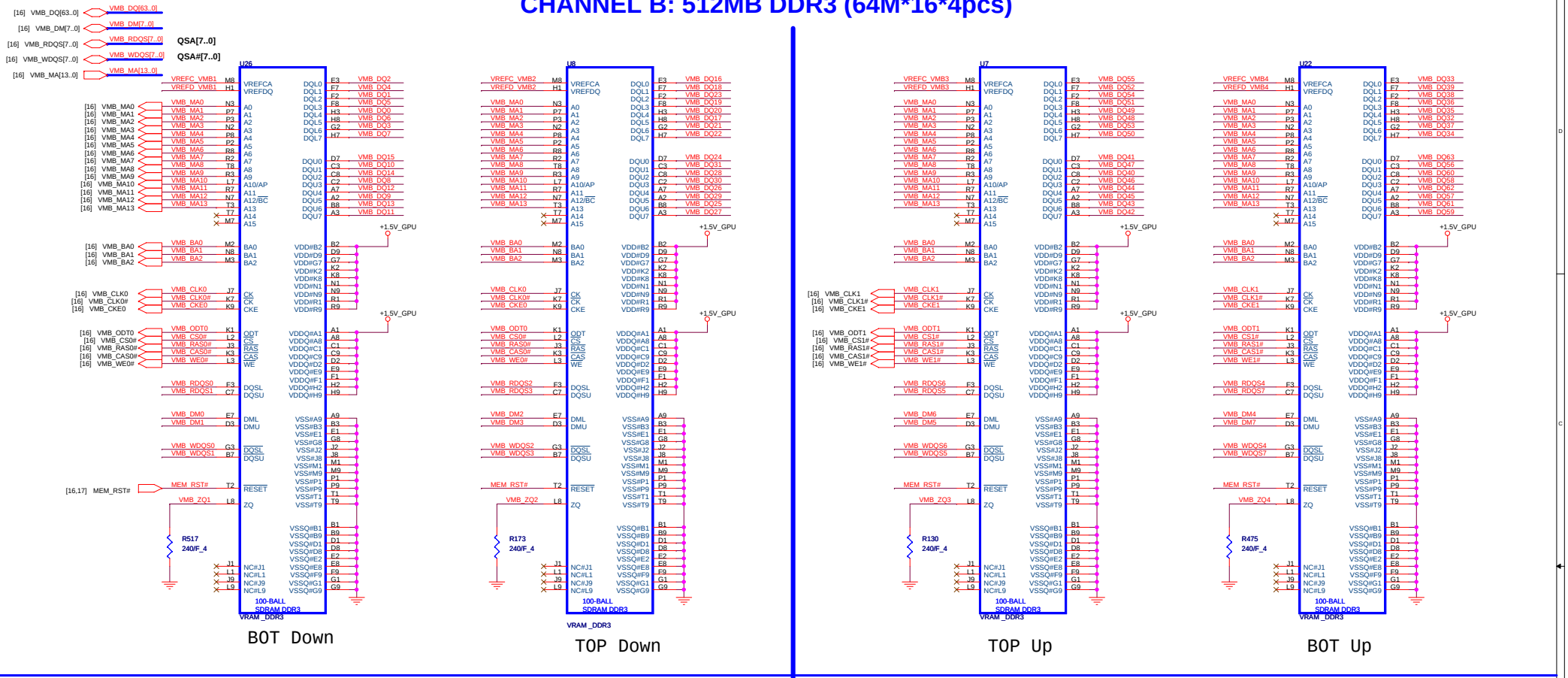
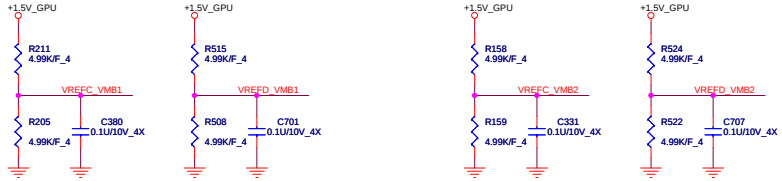
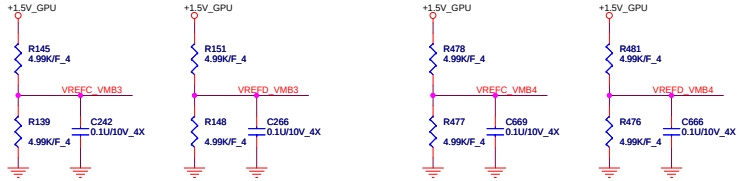
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



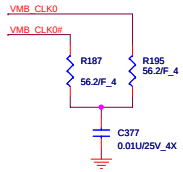
Group-B0 VREF



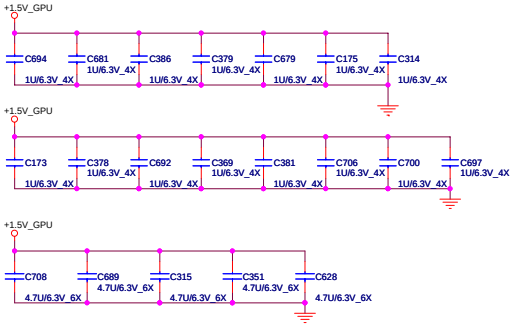
Group-B1 VREF



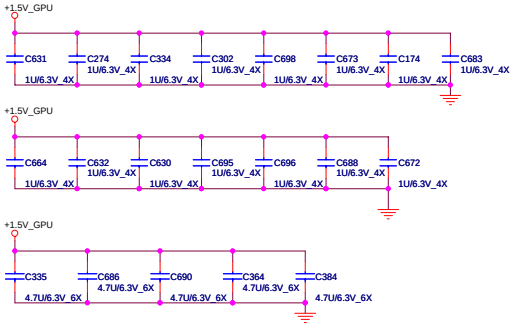
MEM_B0 CLK



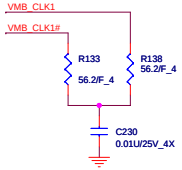
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	2A

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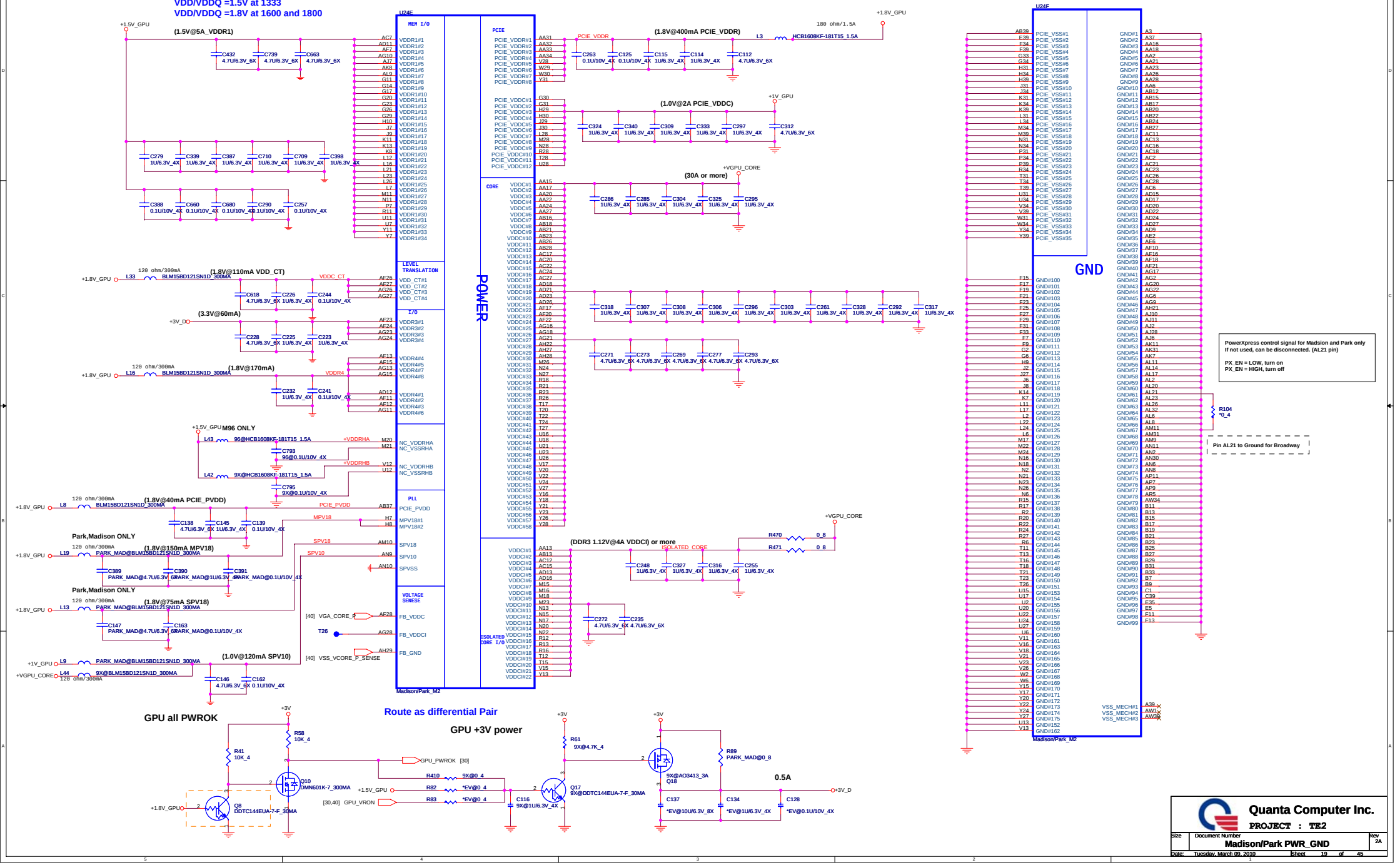
For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Madison/Park PWR_GND	2A

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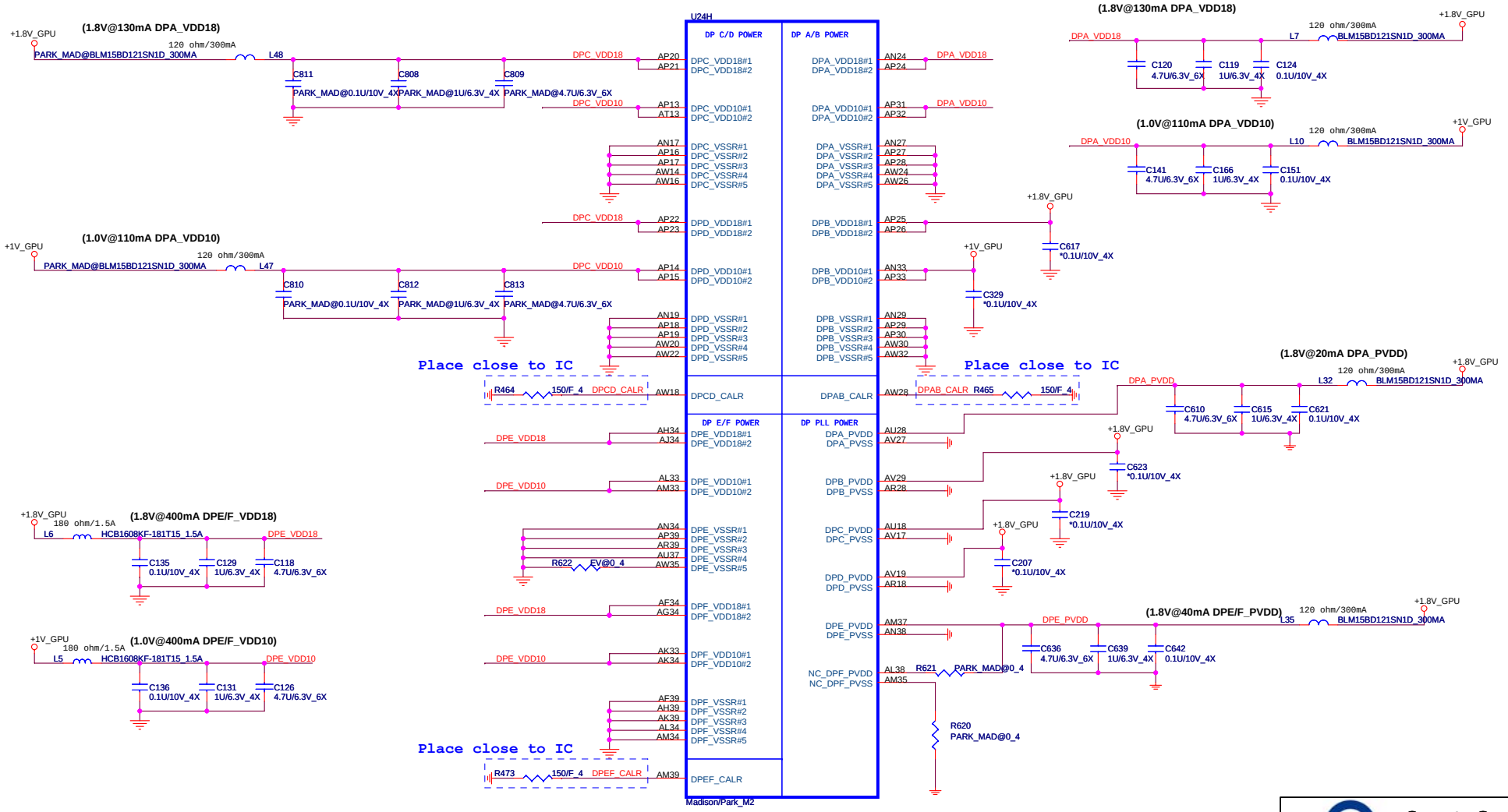

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Madison/Park DPPW_GND	2A

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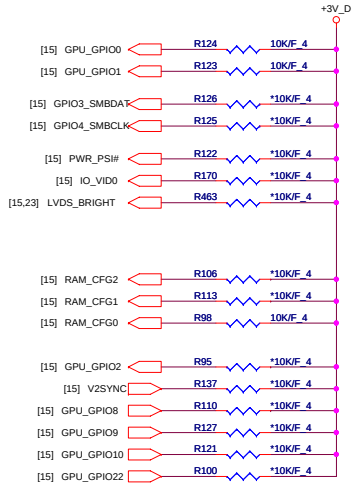
PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

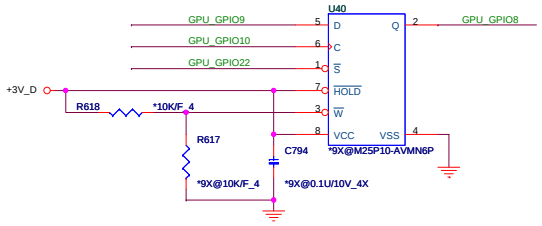
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

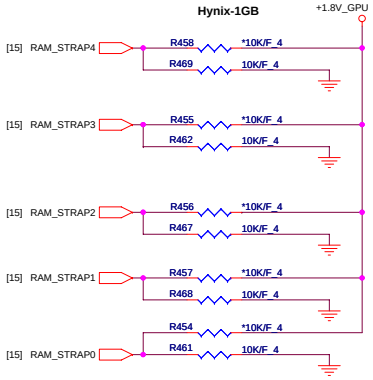
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

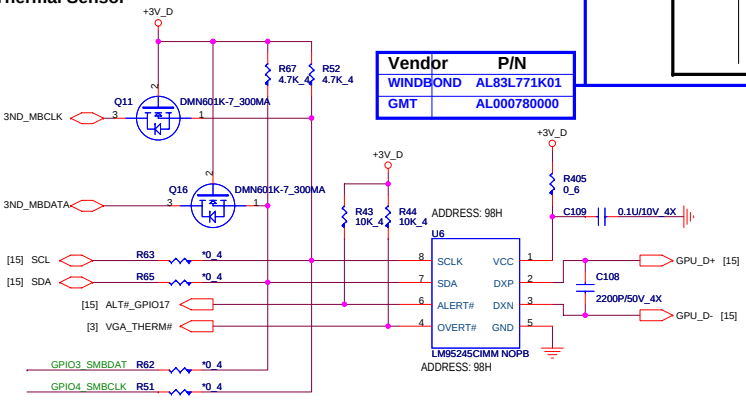


DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
									1

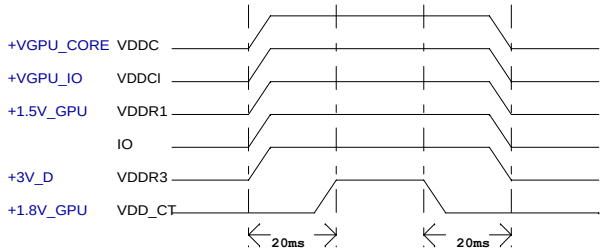


Thermal Sensor



Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

Power Up/Down Sequence



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	2A

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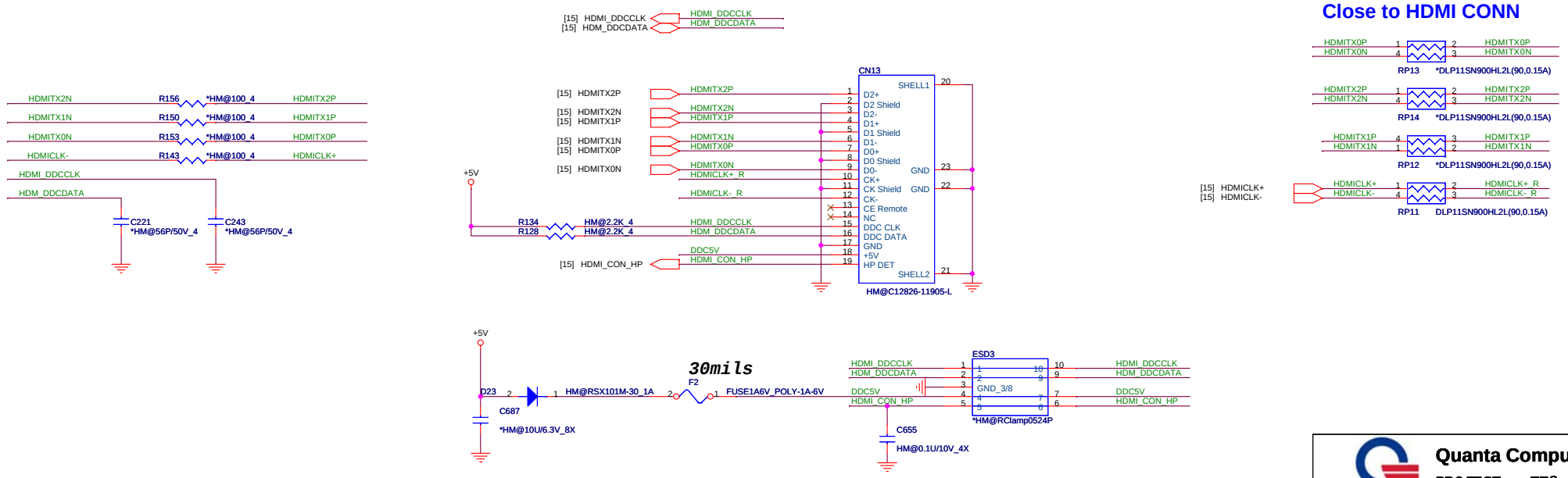
HDMI Conn



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	HDMI CONN	2A

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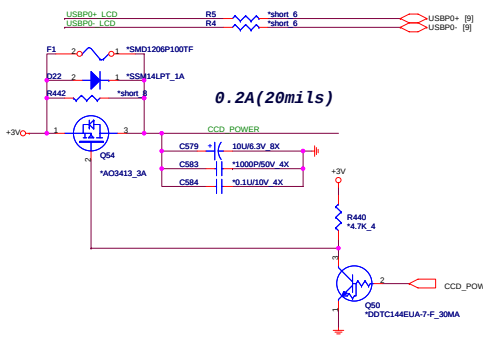
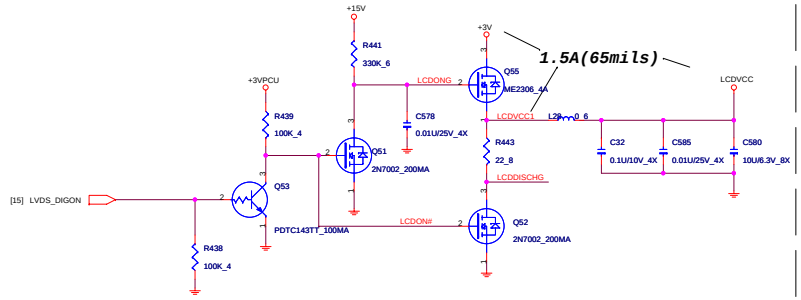
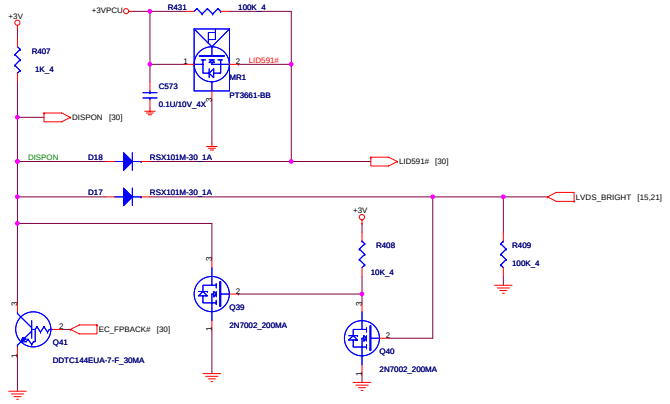
CCD [CCD]



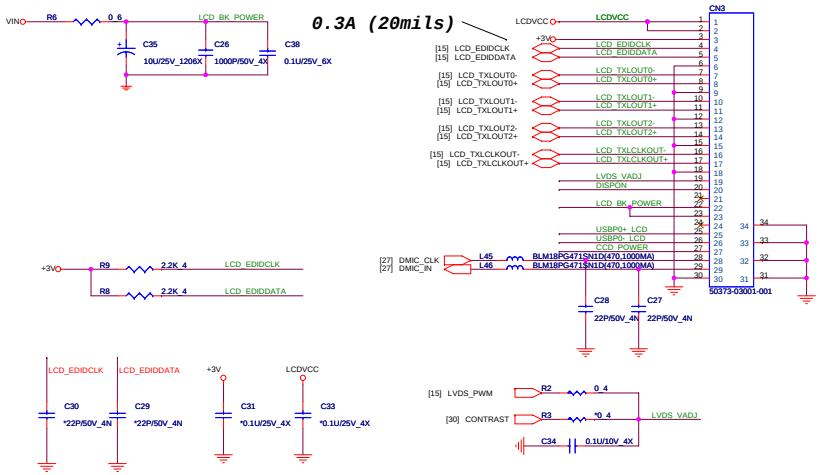
LCD POWER SWITCH [LDS]



HALL SENSOR&BACK LIGHT SWITCH [HSR]

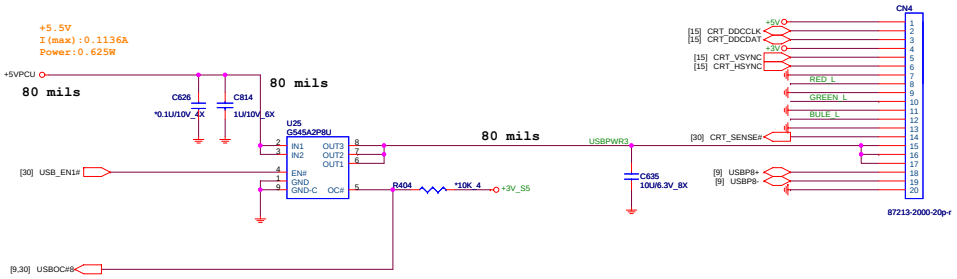


LCD Panel Module [LDS]



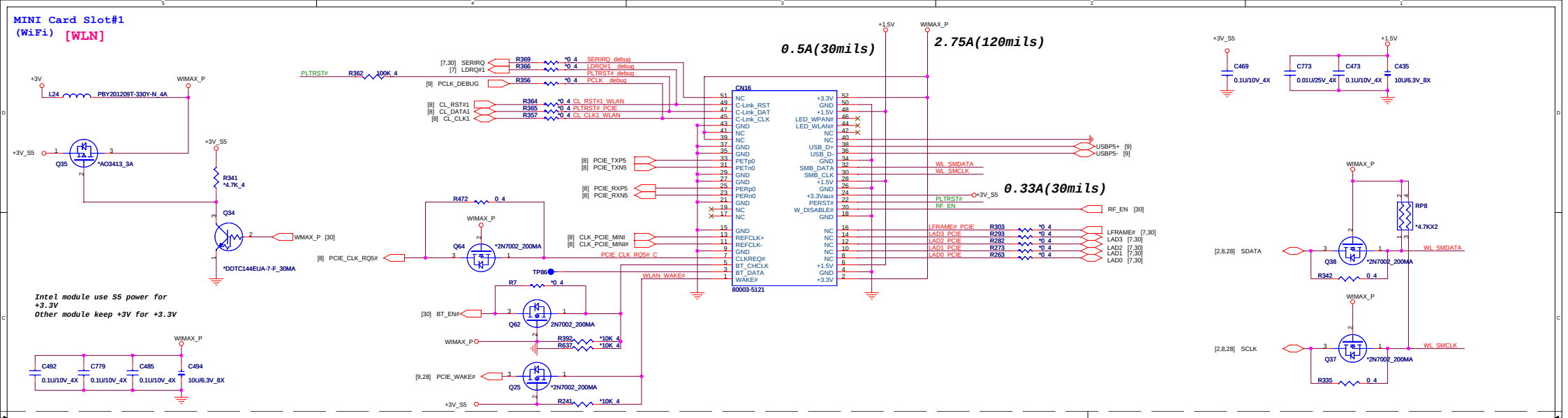
CRT [CRT]

USB To CRT Board [USB]

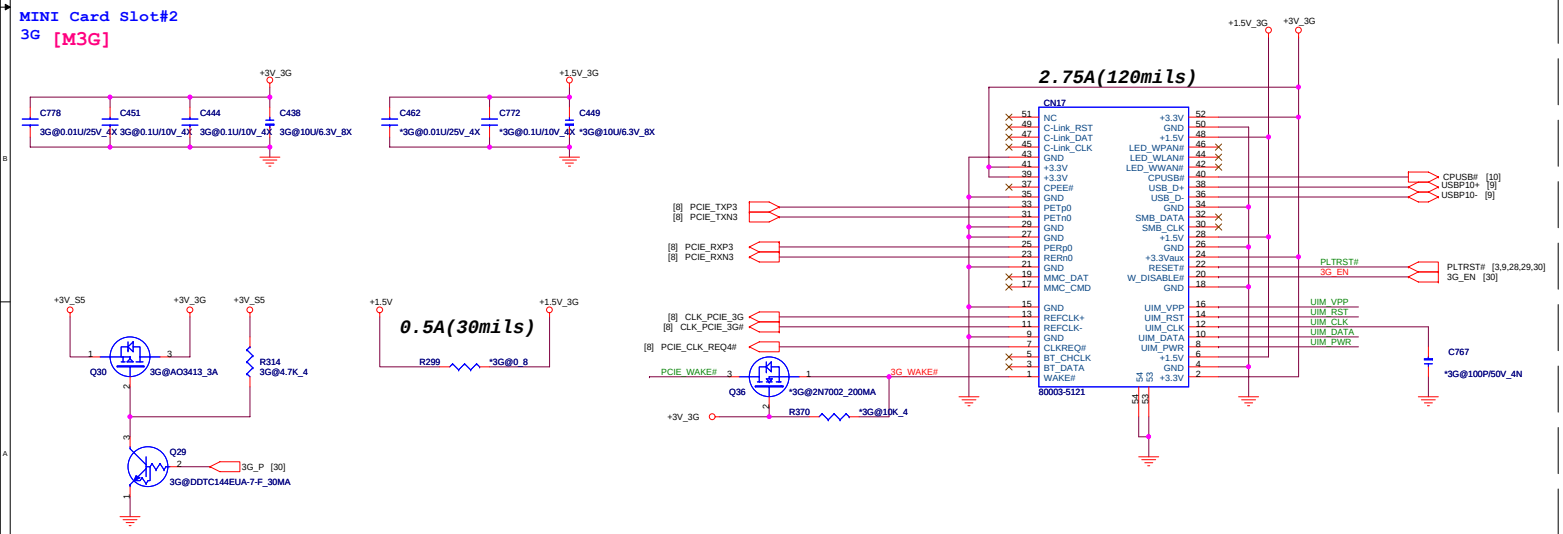


Quanta Computer Inc.	PROJECT : TE2	
Size	Document Number: LCD/LED Panel/CCD	Rev 2A
Date: Tuesday, March 09, 2010	Sheet 23 of 45	

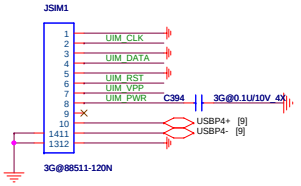
MINI Card Slot#1 (WiFi) [WLN]



MINI Card Slot#2 3G [M3G]



SIM CARD



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	2A

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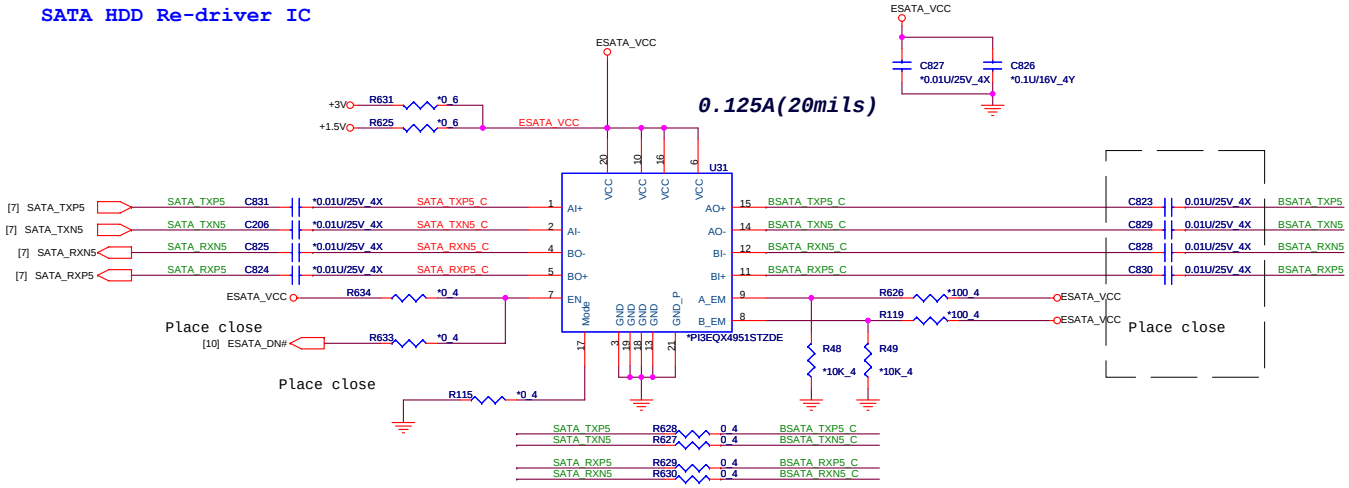
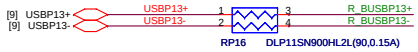
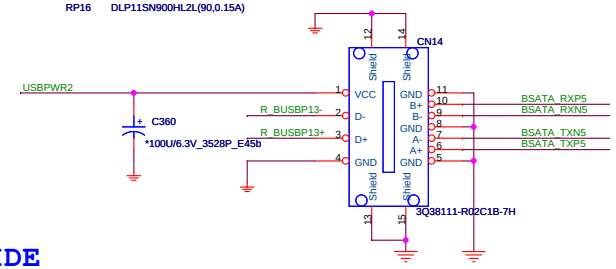
E-SATA [ESA]

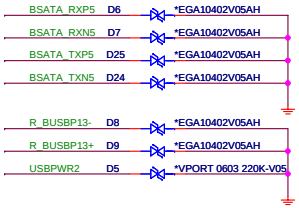
SATA HDD Re-driver IC



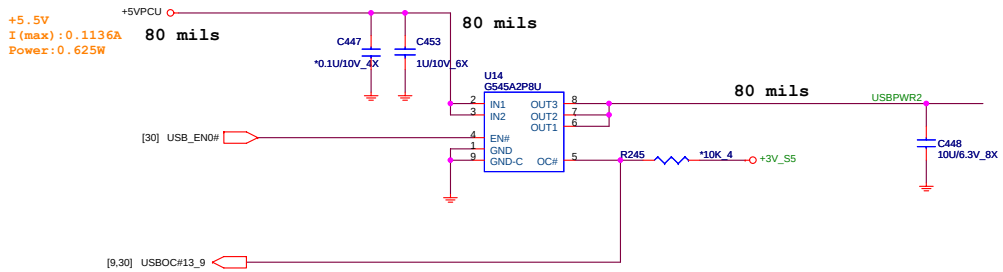


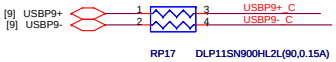
ESATA CONN

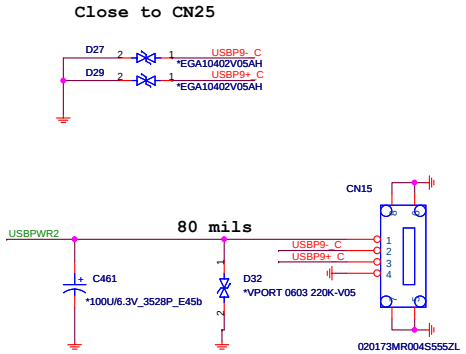




USB MB SIDE







Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	2A

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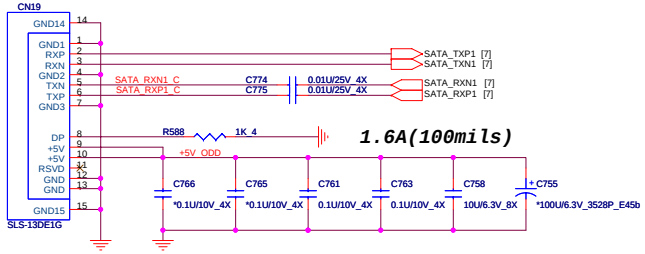
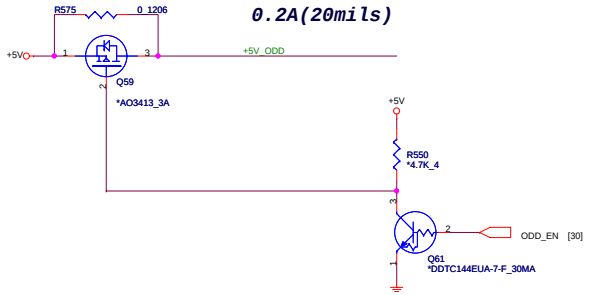
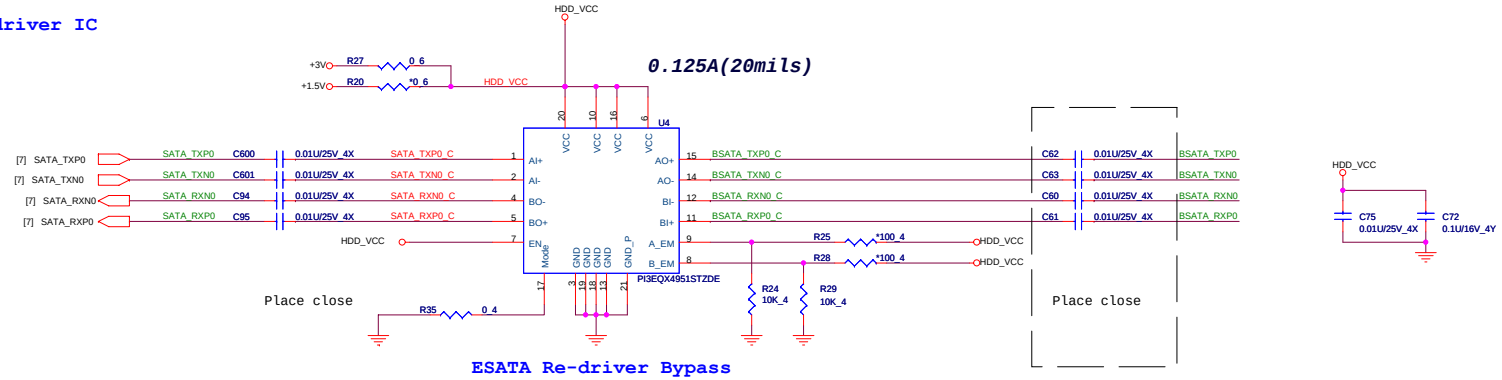
SATA ODD

[ODD]





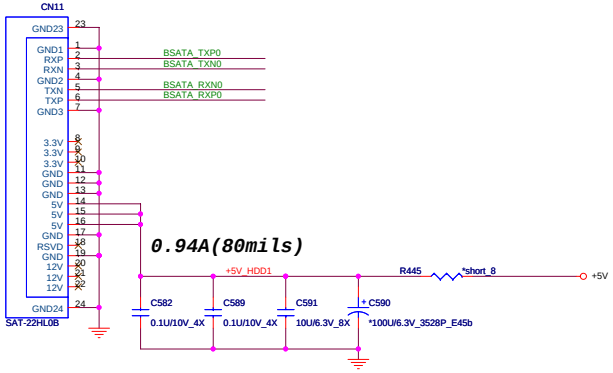
SATA HDD Re-driver IC



ESATA Re-driver Bypass

SATA HDD

[HDD]



Quanta Computer Inc.	PROJECT : TE2	
Size	Document Number: HDD/ODD/MDC	Rev 2A
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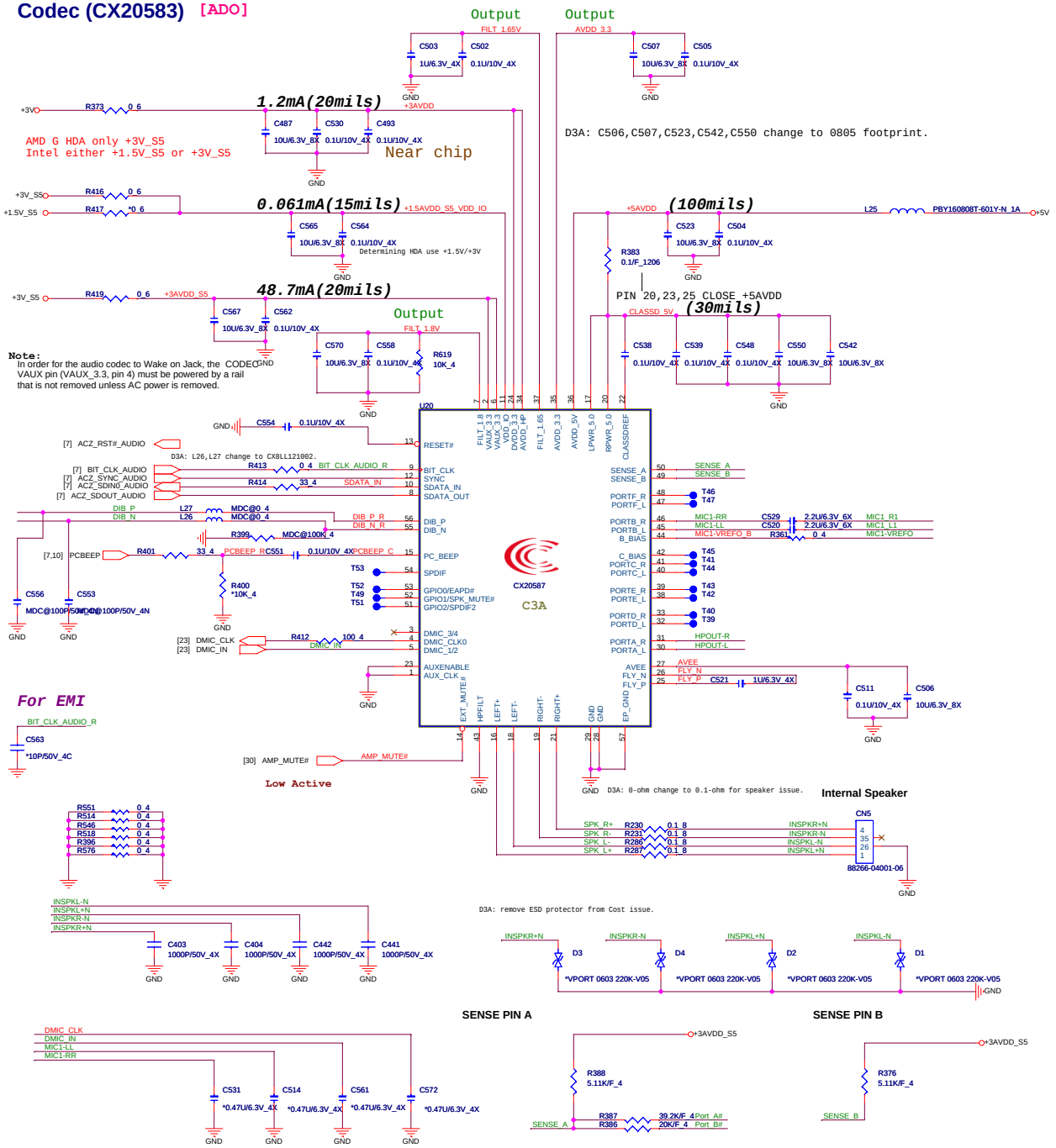
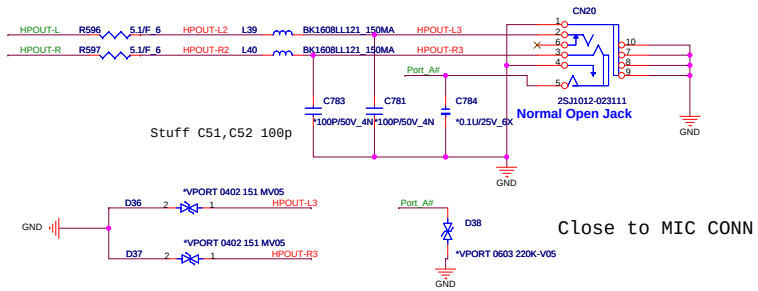
Codec (CX20583) [ADO]

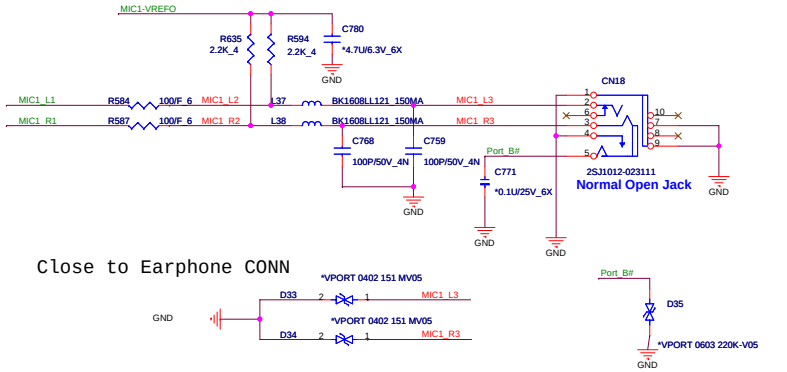


AUDIO JACK

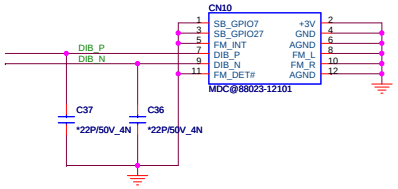
Earphone



External MIC



MDC



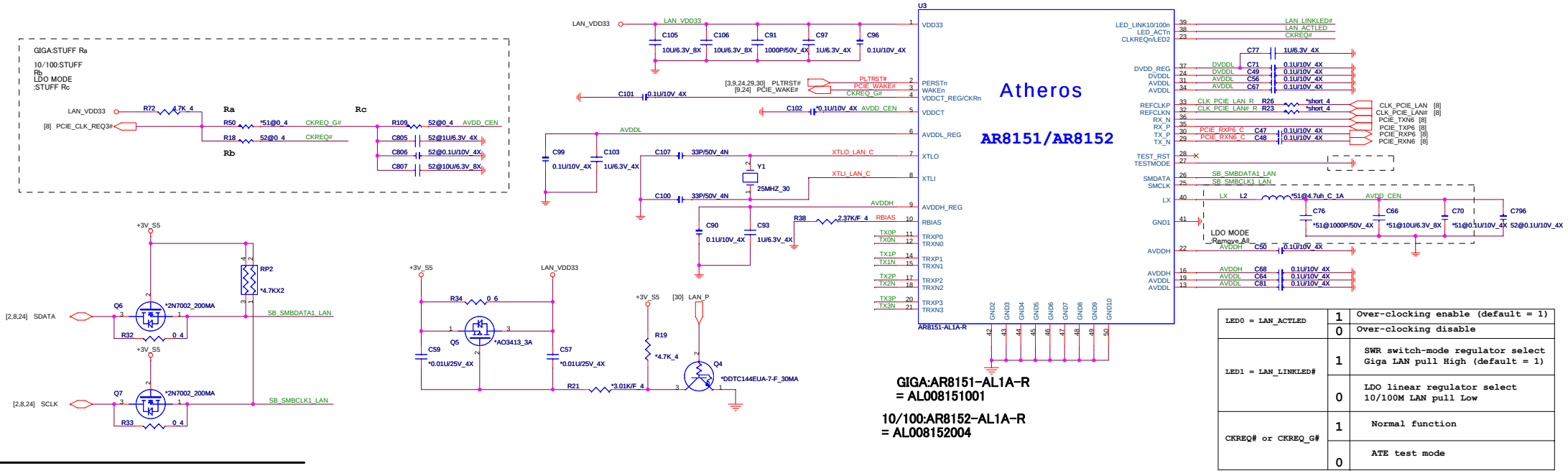
Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Codec (CX20583)	2A

Date: Friday, March 19, 2010 Sheet 27 of 45

Atheros Lan

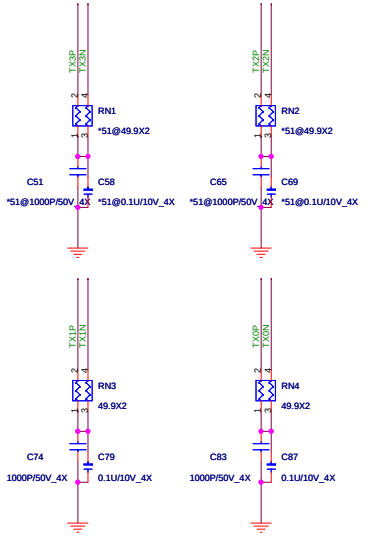


GIGA:AR8151-AL1A-R
= AL008151001

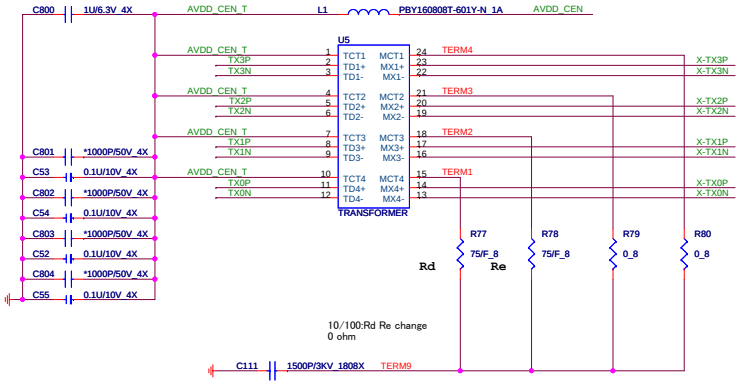
10/100:AR8152-AL1A-R
= AL008152004

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

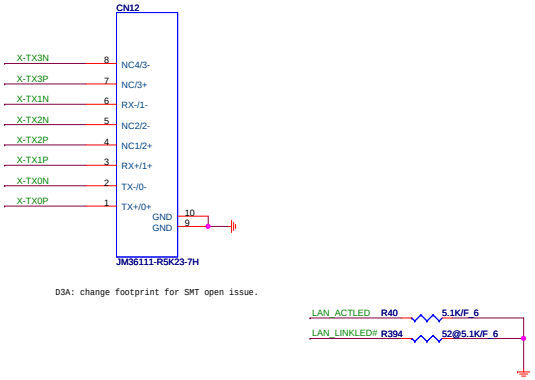
PLACE NEAR LAN IC SIDE



TRANSFORMER



RJ45



D3A: change footprint for SMT open issue.

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Atheros Lan	2A

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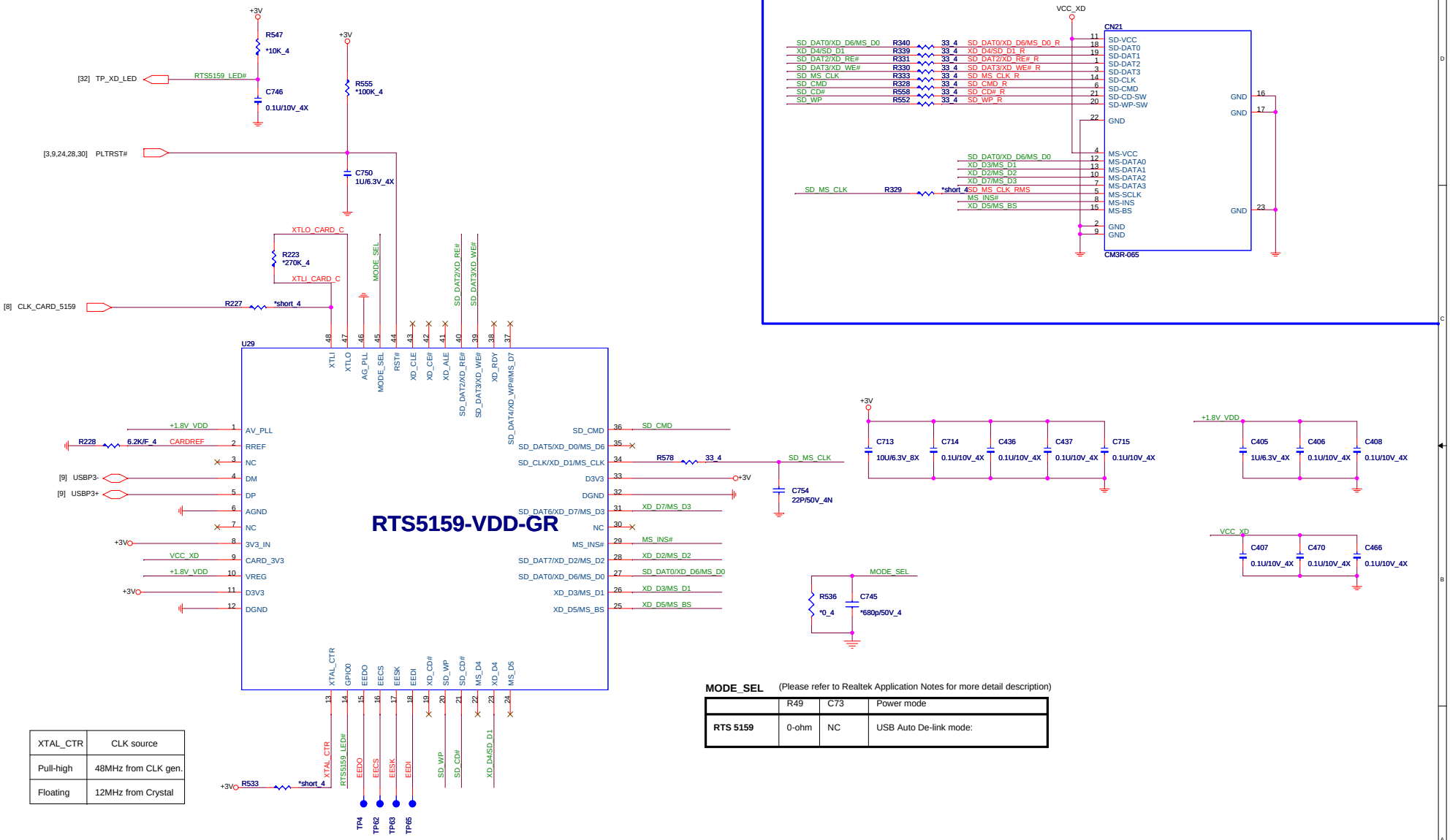
3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

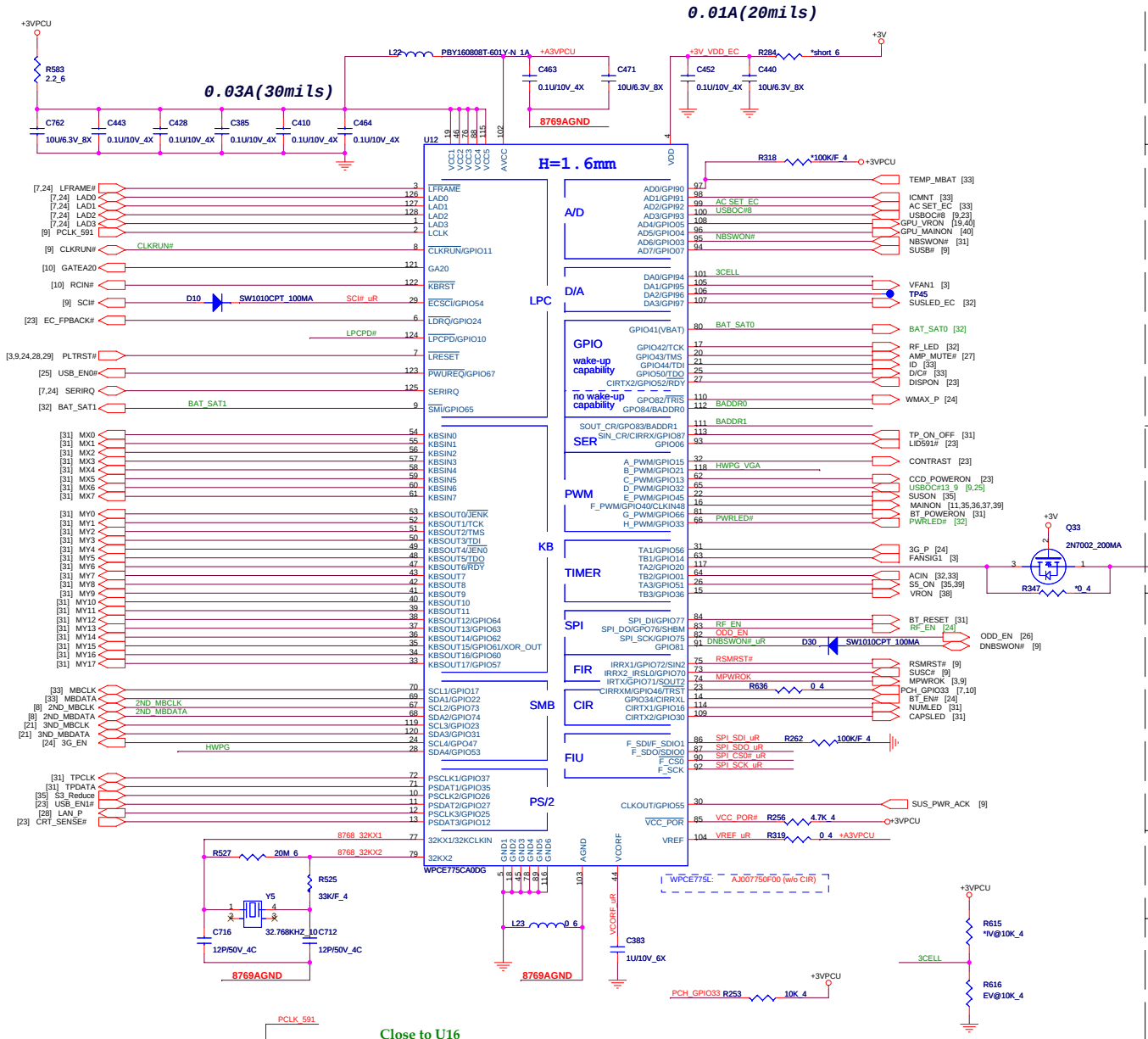
Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	RTS5159 (Card Reader)	2A

Date: Tuesday, March 09, 2010 Sheet 29 of 45

EC [KBC]



SM BUS PU

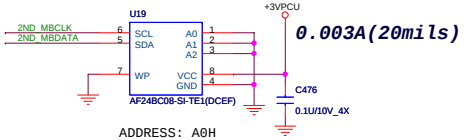
I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

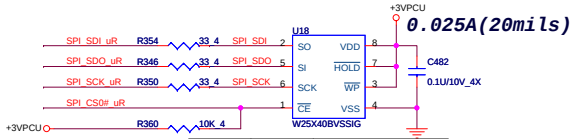
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

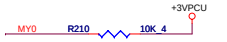


SPI FLASH

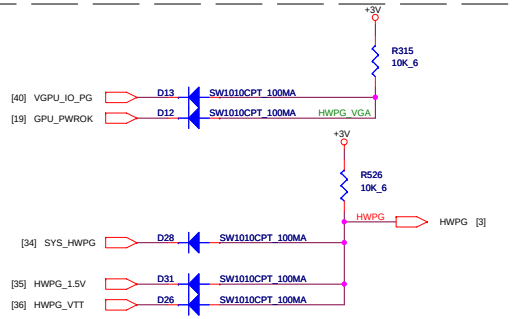


Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET



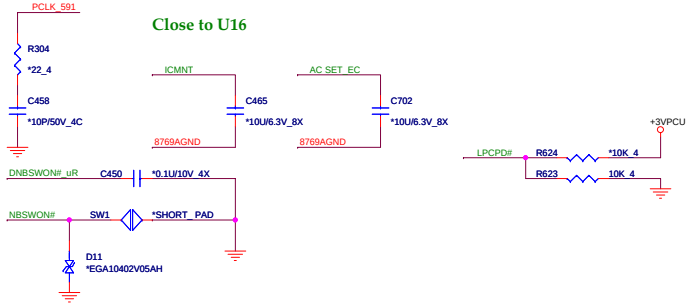
HWPG



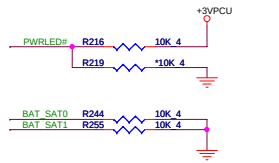
SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

Close to U16



LED PU/PD



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	EC-WPC8763LDG/WPC8769L(O)	2A

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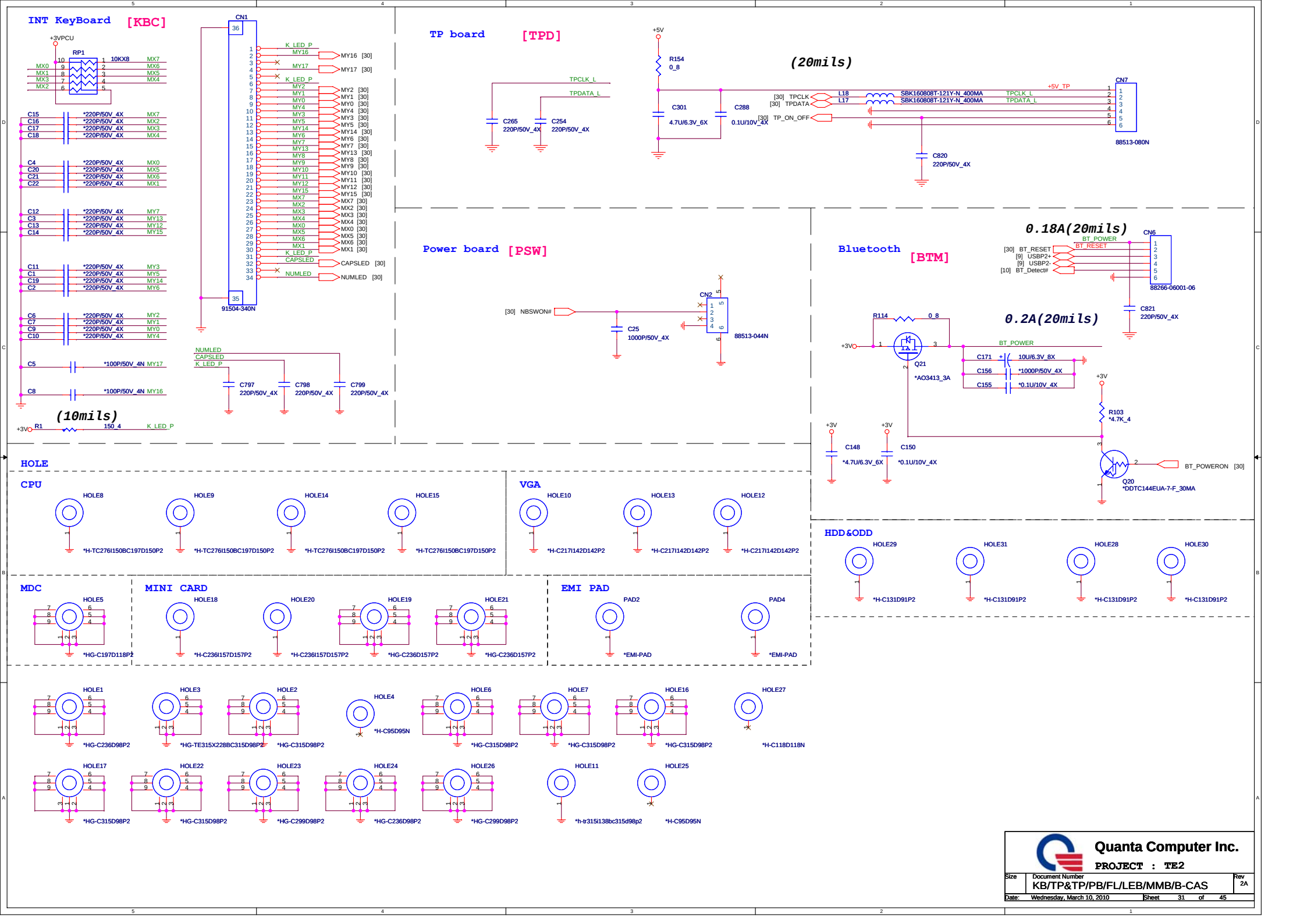
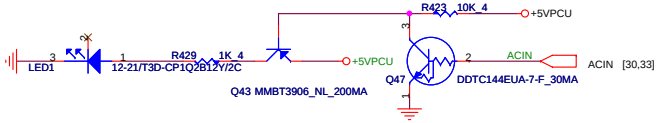

INT KeyBoard [KBC]
+3VPCU
RP1
10KX8
MX0
MX1
MX3
MX2
MX7
MX6
MX5
MX4
C15 *220P/50V_4X MX7
C16 *220P/50V_4X MX2
C17 *220P/50V_4X MX3
C18 *220P/50V_4X MX4
C4 *220P/50V_4X MX0
C20 *220P/50V_4X MX5
C21 *220P/50V_4X MX6
C22 *220P/50V_4X MX1
C12 *220P/50V_4X MY7
C3 *220P/50V_4X MY13
C13 *220P/50V_4X MY12
C14 *220P/50V_4X MY15
C11 *220P/50V_4X MY3
C1 *220P/50V_4X MY5
C19 *220P/50V_4X MY14
C2 *220P/50V_4X MY6
C6 *220P/50V_4X MY2
C7 *220P/50V_4X MY1
C9 *220P/50V_4X MY0
C10 *220P/50V_4X MY4
C5 *100P/50V_4N MY17
C8 *100P/50V_4N MY16
(10mils)
+3V R1 150_4 K_LED_P
CN1
91504-340N
K_LED_P
MY16 [30]
MY17 [30]
K_LED_P
MY2 [30]
MY1 [30]
MY0 [30]
MY4 [30]
MY3 [30]
MY5 [30]
MY14 [30]
MY6 [30]
MY7 [30]
MY13 [30]
MY8 [30]
MY9 [30]
MY10 [30]
MY11 [30]
MY12 [30]
MY15 [30]
MX7 [30]
MX2 [30]
MX3 [30]
MX4 [30]
MX0 [30]
MX5 [30]
MX6 [30]
MX1 [30]
K_LED_P
CAPSLED
CAPSLED [30]
NUMLED
NUMLED [30]
NUMLED
CAPSLED
K_LED_P
C797 220P/50V_4X
C798 220P/50V_4X
C799 220P/50V_4X
TP board [TPD]
+5V
R154 0_8
(20mils)
TPCLK_L
TPDATA_L
C265 220P/50V_4X
C254 220P/50V_4X
C301 4.7U/6.3V_6X
C288 0.1U/10V_4X
[30] TPCLK
[30] TPDATA
[30] TP_ON_OFF
L18 SBK160808T-121Y-N_400MA
L17 SBK160808T-121Y-N_400MA
TPCLK_L
TPDATA_L
+5V_TP
CN7
88513-080N
C820 220P/50V_4X
Power board [PSW]
[30] NBSWON#
C25 1000P/50V_4X
CN2
88513-044N
Bluetooth [BTM]
0.18A(20mils)
BT_POWER
BT_RESET
[30] BT_RESET
[9] USBP2+
[9] USBP2-
[10] BT_Detect#
CN6
88266-06001-06
C821 220P/50V_4X
R114 0_8
0.2A(20mils)
+3V
Q21
*AO3413_3A
BT_POWER
C171 10U/6.3V_8X
C156 *1000P/50V_4X
C155 *0.1U/10V_4X
R103 *4.7K_4
C148 *4.7U/6.3V_6X
C150 *0.1U/10V_4X
BT_POWERON [30]
Q20 *DDTC144EUA-7-F_30MA
HOLE
CPU
HOLE8 *H-TC276I150BC197D150P2
HOLE9 *H-TC276I150BC197D150P2
HOLE14 *H-TC276I150BC197D150P2
HOLE15 *H-TC276I150BC197D150P2
VGA
HOLE10 *H-C217I142D142P2
HOLE13 *H-C217I142D142P2
HOLE12 *H-C217I142D142P2
HDD&ODD
HOLE29 *H-C131D91P2
HOLE31 *H-C131D91P2
HOLE28 *H-C131D91P2
HOLE30 *H-C131D91P2
MDC
HOLE5 *HG-C197D118P2
MINI CARD
HOLE18 *H-C236I157D157P2
HOLE20 *H-C236I157D157P2
HOLE19 *HG-C236D157P2
HOLE21 *HG-C236D157P2
EMI PAD
PAD2 *EMI-PAD
PAD4 *EMI-PAD
HOLE1 *HG-C236D98P2
HOLE3 *HG-TE315X228BC315D98P2
HOLE2 *HG-C315D98P2
HOLE4 *H-C95D95N
HOLE6 *HG-C315D98P2
HOLE7 *HG-C315D98P2
HOLE16 *HG-C315D98P2
HOLE27 *H-C118D118N
HOLE17 *HG-C315D98P2
HOLE22 *HG-C315D98P2
HOLE23 *HG-C299D98P2
HOLE24 *HG-C236D98P2
HOLE26 *HG-C299D98P2
HOLE11 *h-tr315i138bc315d98p2
HOLE25 *H-C95D95N
Quanta Computer Inc.
PROJECT : TE2
Size
Document Number
KB/TP&TP/PB/FL/LEB/MMB/B-CAS
Rev 2A
Date: Wednesday, March 10, 2010
Sheet 31 of 45

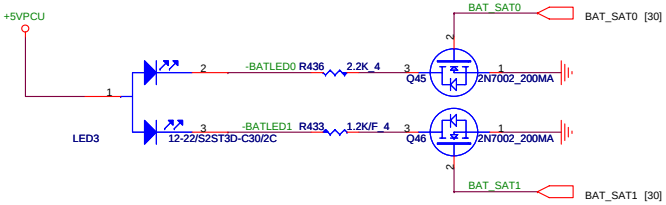
LED [LED]

AC-IN



BATERRY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

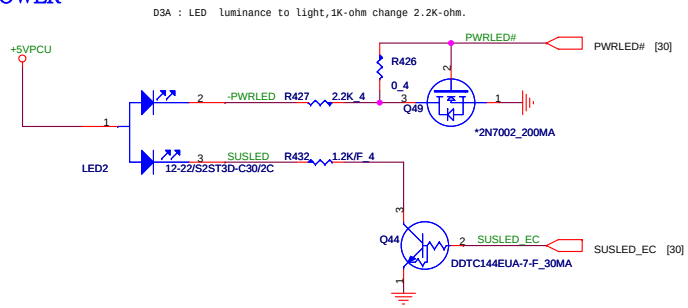


RF LED

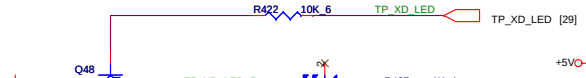
D3A : LED luminance to light,560-ohm change 220-ohm.

POWER

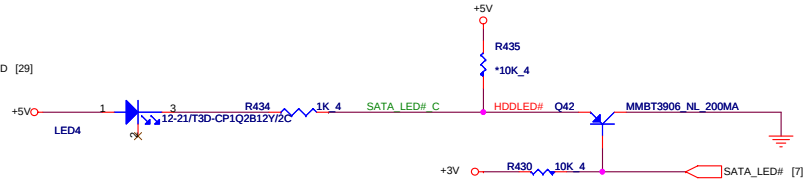
D3A : LED luminance to light,1K-ohm change 2.2K-ohm.



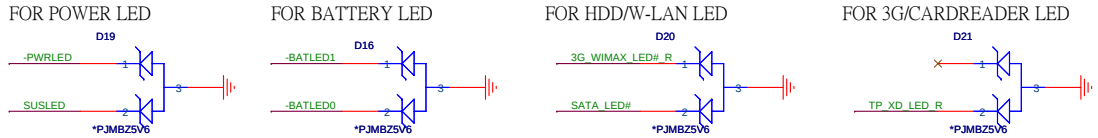
CARDREADER

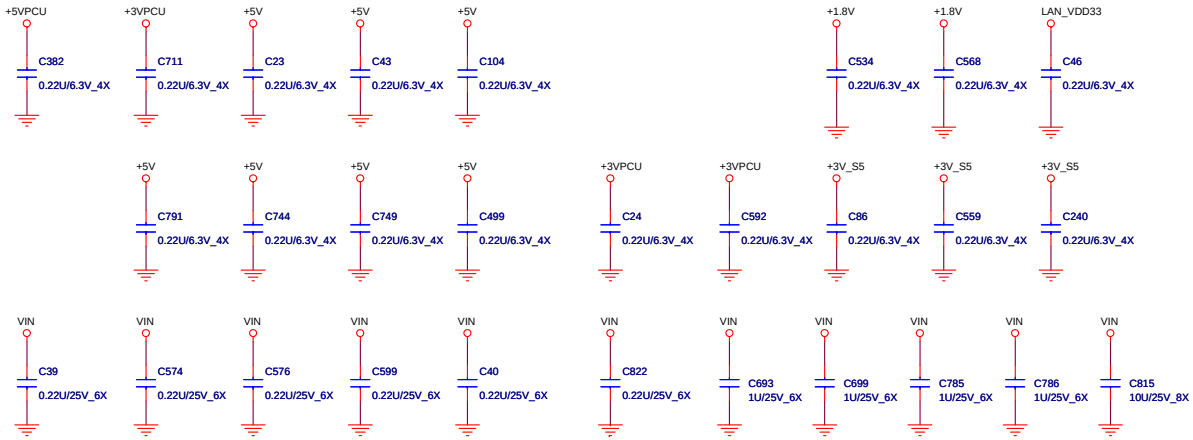


HDD/ODD

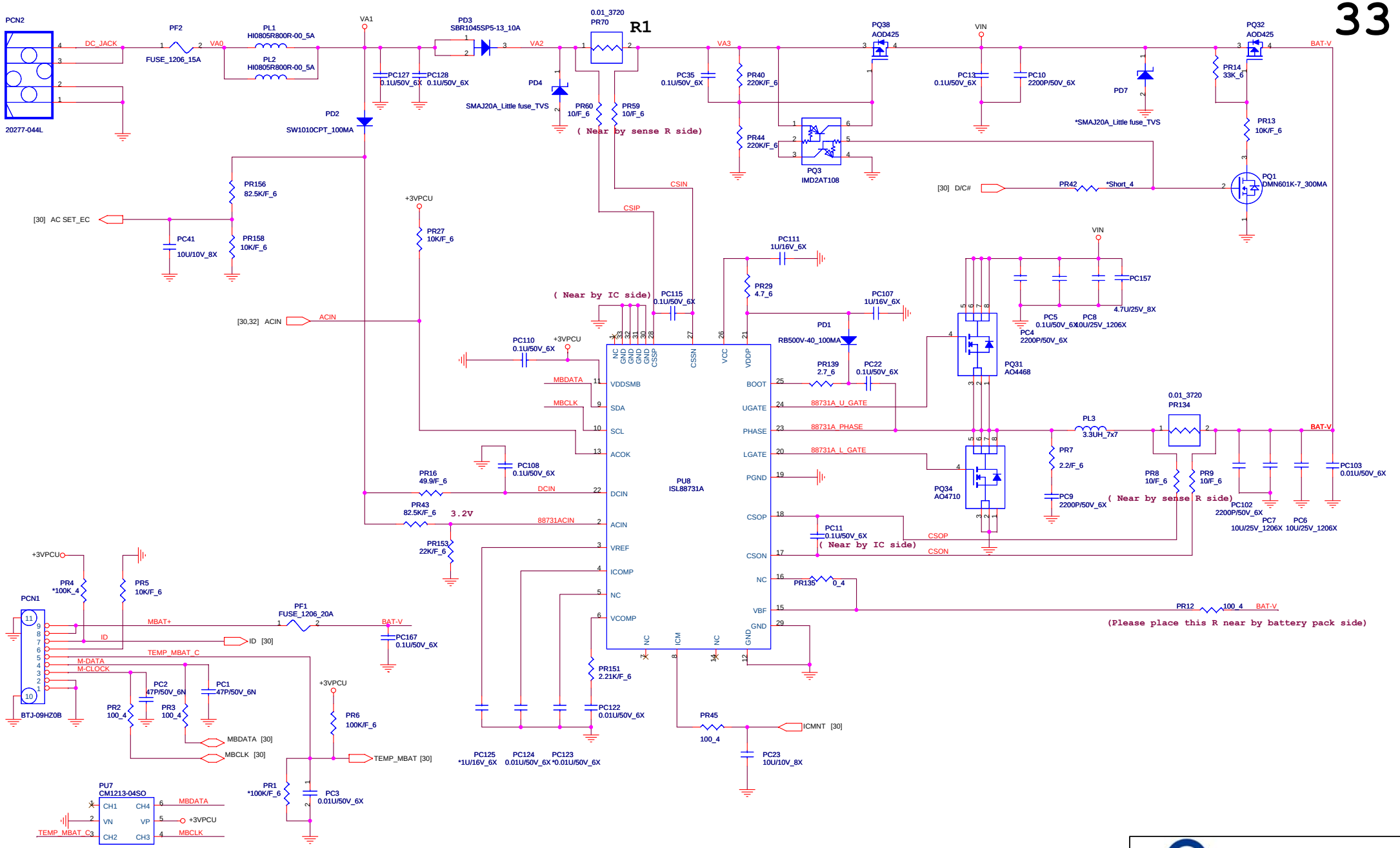


ESD Protect





Quanta Computer Inc.	PROJECT : TE2	
Size	Document Number: LED/HOLE	Rev 2A
Date: Tuesday, March 09, 2010	Sheet 32 of 45	

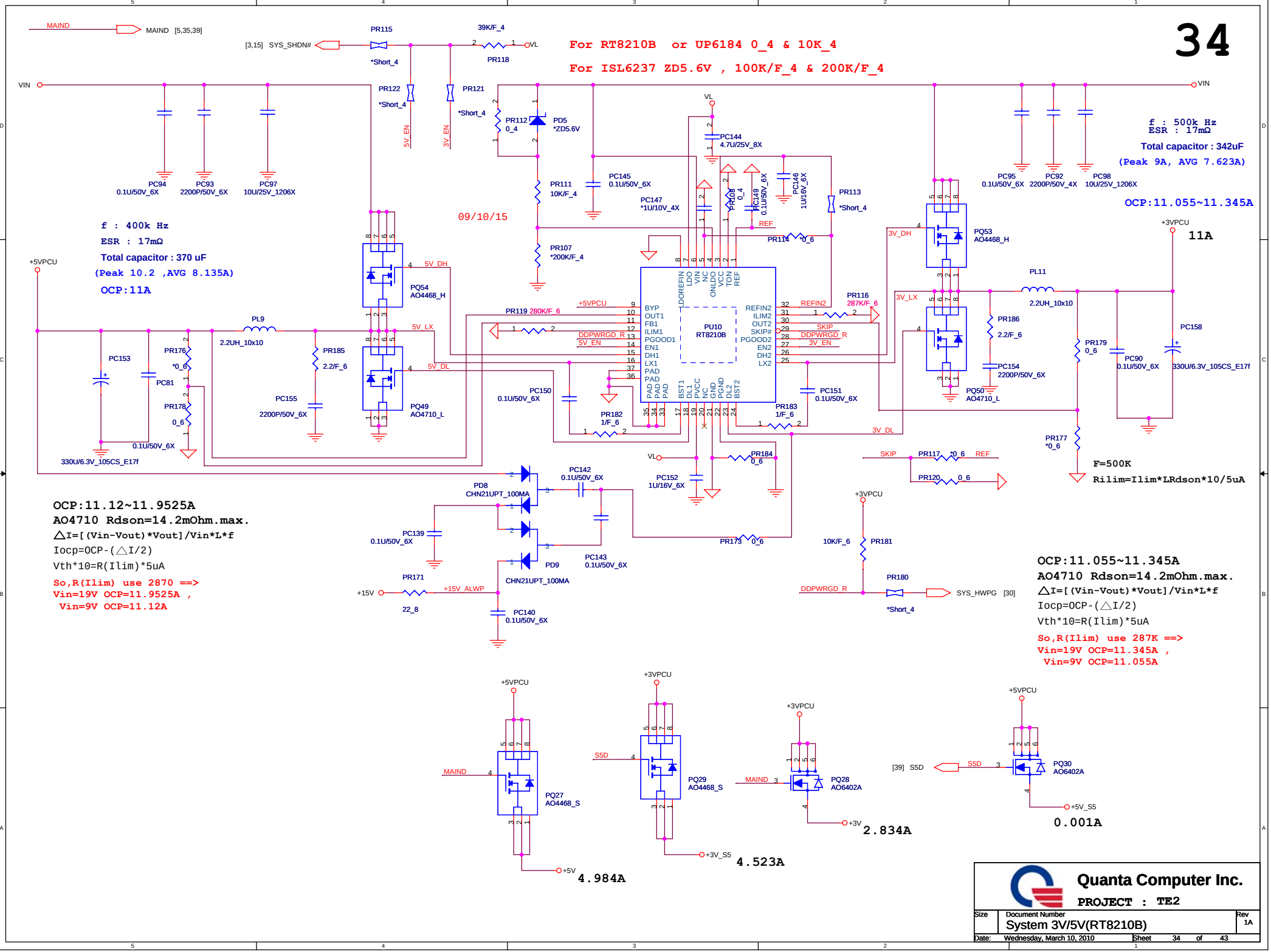


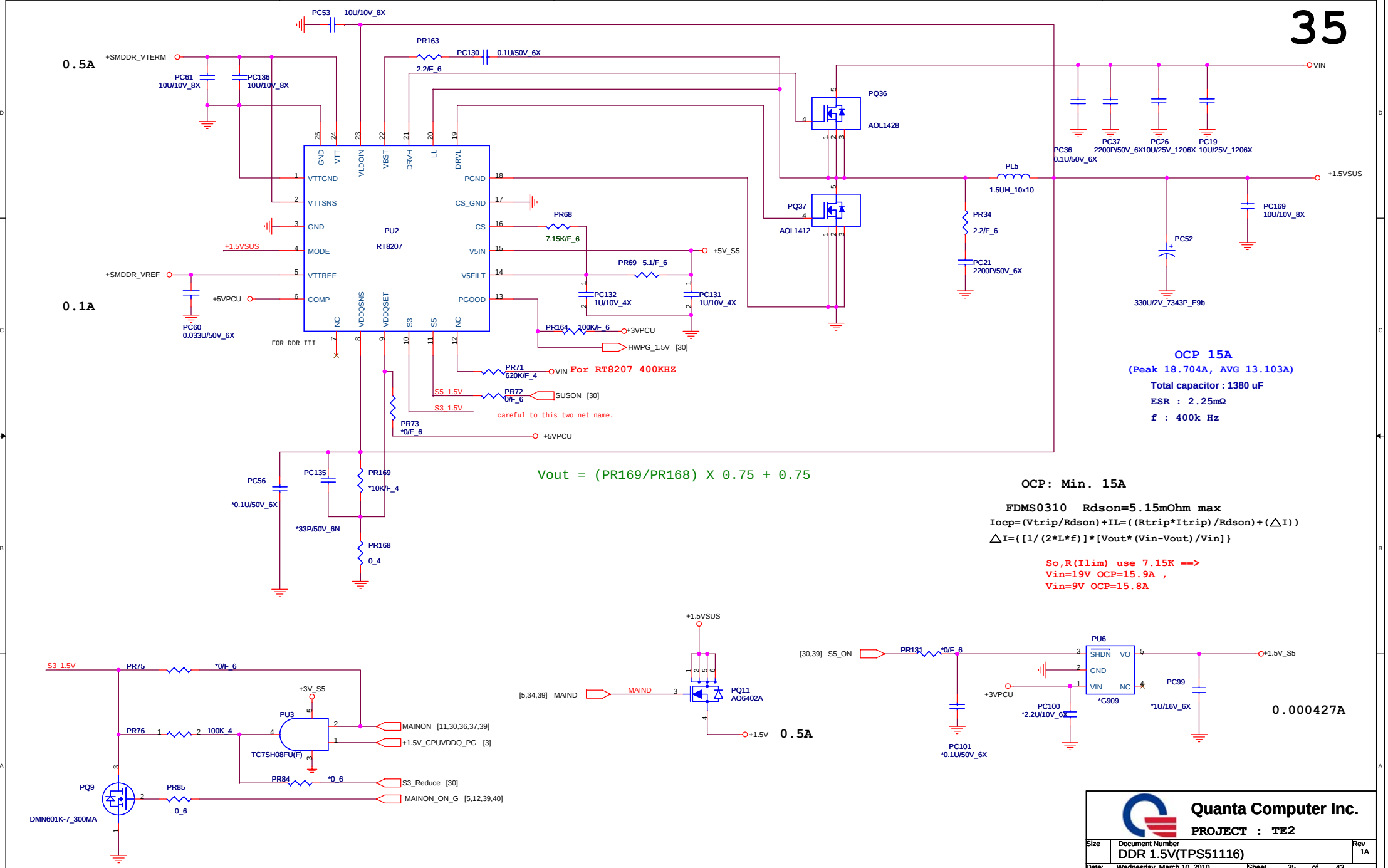
Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Charger (ISL88731)	1A

Date: Wednesday, March 10, 2010 Sheet 33 of 43


For RT8210B or UP6184 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4
09/10/15
f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 10.2 ,AVG 8.135A)
OCP:11A
f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 9A, AVG 7.623A)
OCP:11.055~11.345A
11A
F=500K
Rilim=Ilim*LRdson*10/5uA
OCP:11.12~11.9525A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 2870 ==>
Vin=19V OCP=11.9525A ,
Vin=9V OCP=11.12A
OCP:11.055~11.345A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 287K ==>
Vin=19V OCP=11.345A ,
Vin=9V OCP=11.055A
4.984A
4.523A
2.834A
0.001A
Quanta Computer Inc.
PROJECT : TE2
System 3V/5V(RT8210B)
Rev 1A
Date: Wednesday, March 10, 2010
Sheet 34 of 43

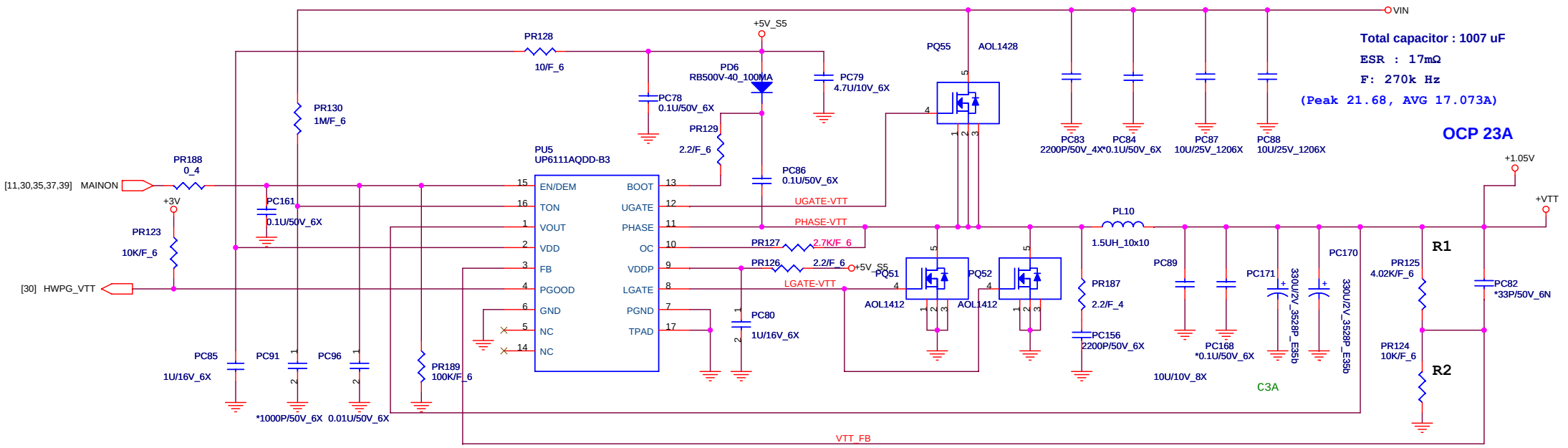


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Wednesday, March 10, 2010 Sheet 35 of 43



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

OCP:23.18~23.27A

FDMS0310 Rdson=5.15mOhm max

Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))

△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}

Rdson*OCP=RIlim*20uA

So,R(Ilim) use 2.7K ==>
Vin=19V OCP=23.18A ,
Vin=9V OCP=23.27A

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	+VTT (UP6111A)	1A

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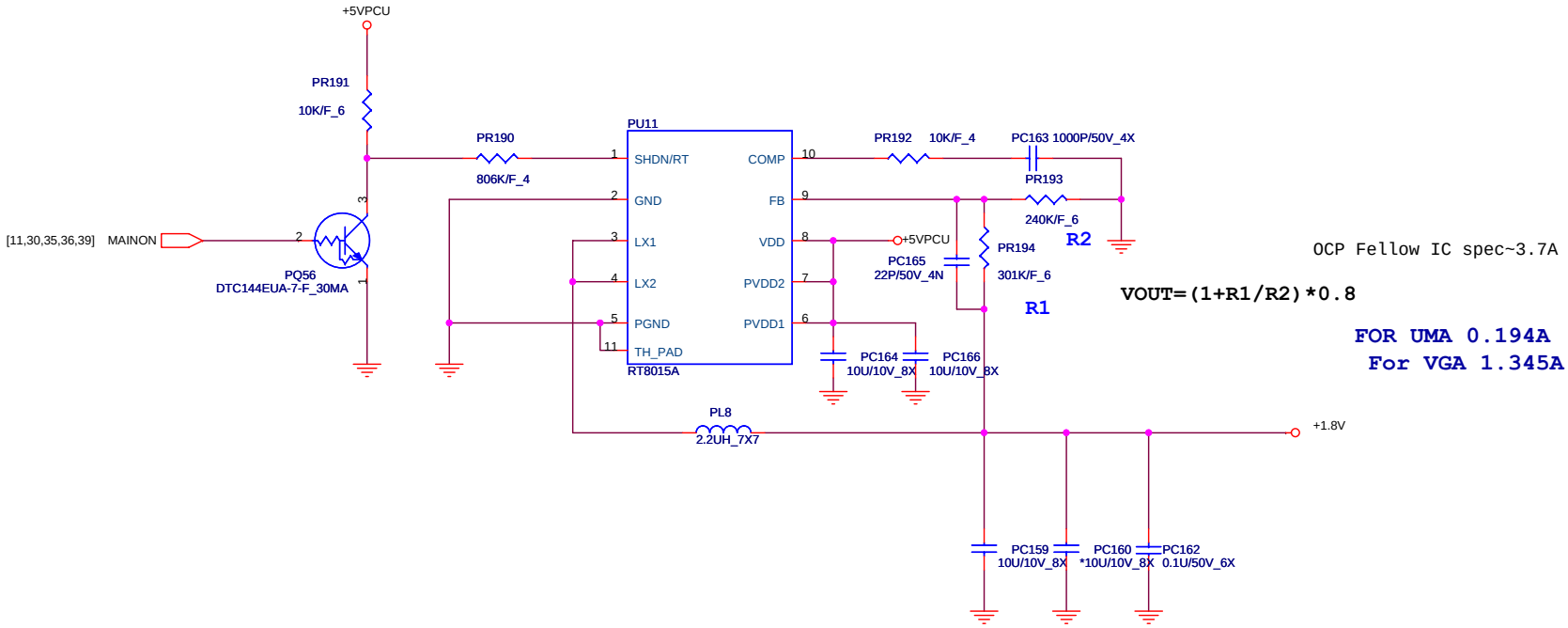


OCP Fellow IC spec~3.7A

VOUT=(1+R1/R2)*0.8

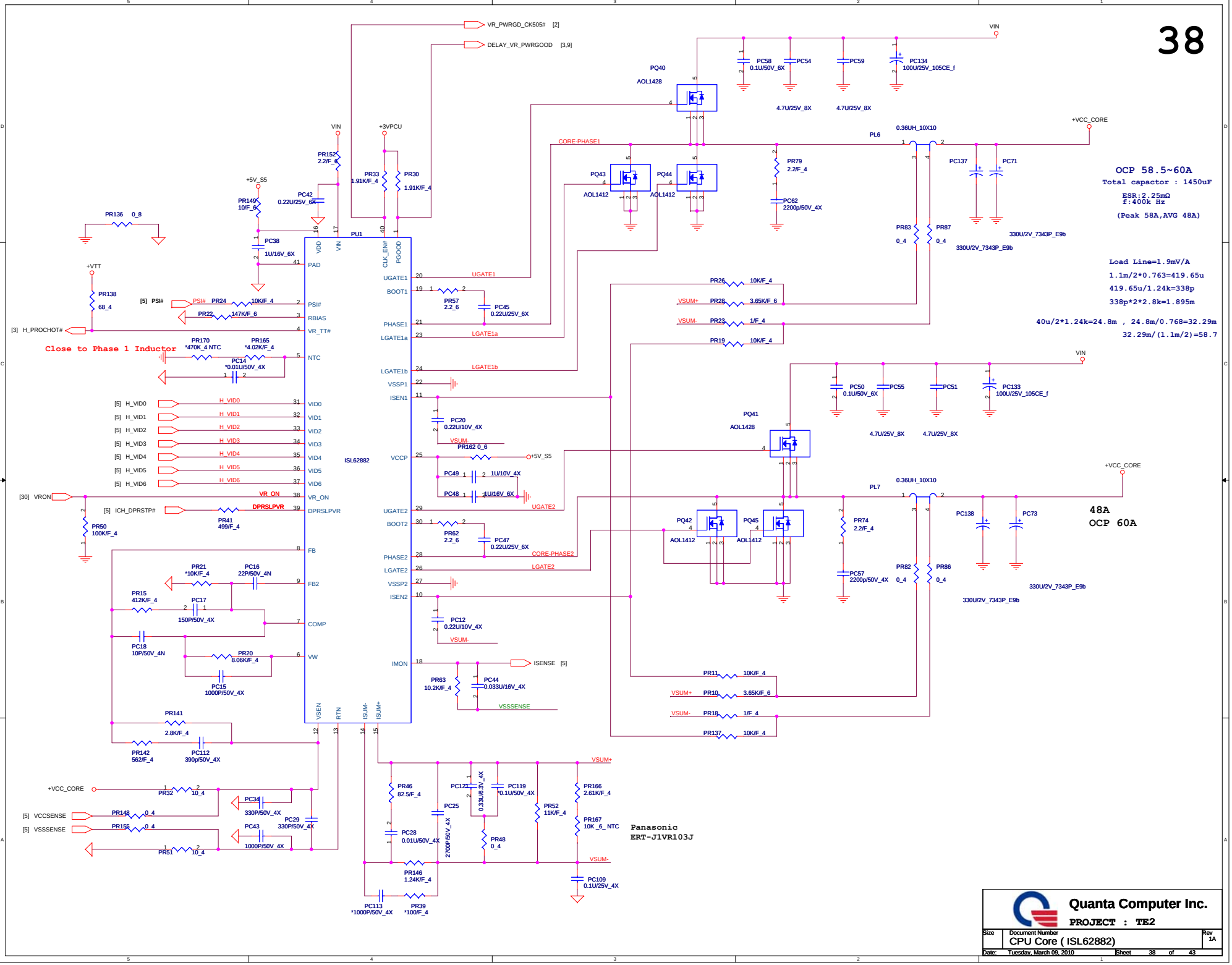
FOR UMA 0.194A
For VGA 1.345A

Quanta Computer Inc.

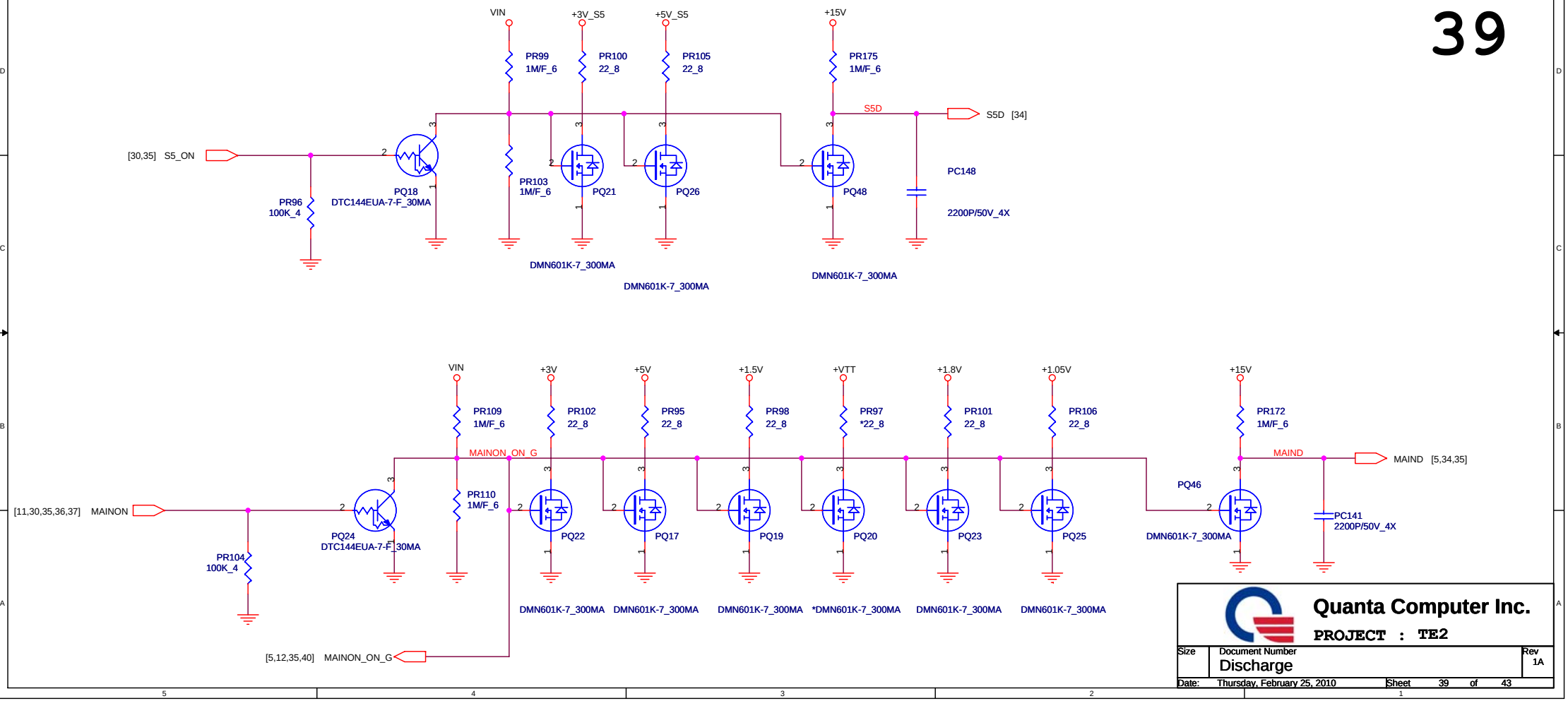
PROJECT : TE2

Size	Document Number	Rev
	+1.8V (RT8015A)	1A

Date: Wednesday, March 10, 2010 Sheet 37 of 43



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: CPU Core (ISL62882)	Rev 1A
Date: Tuesday, March 09, 2010	Sheet 38 of 43	

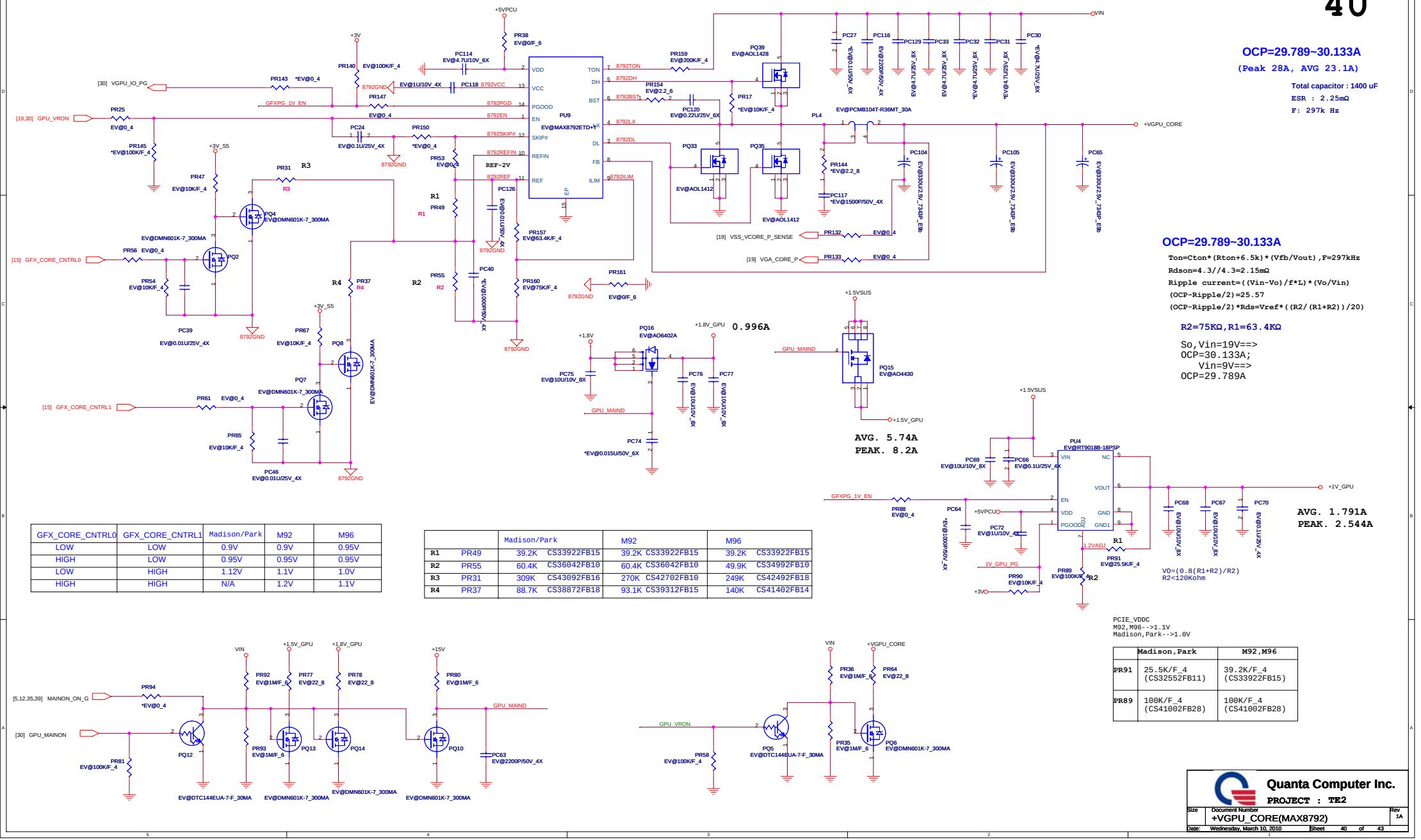


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Discharge	1A

Date: Thursday, February 25, 2010 Sheet 39 of 43



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	Madison/Park	M92	M96
LOW	LOW	0.9V	0.9V	0.95V
HIGH	LOW	0.95V	0.95V	0.95V
LOW	HIGH	1.12V	1.1V	1.0V
HIGH	HIGH	N/A	1.2V	1.1V

		Madison/Park		M92		M96	
R1	PR49	39.2K	CS33922FB15	39.2K	CS33922FB15	39.2K	CS33922FB15
R2	PR55	60.4K	CS36042FB10	60.4K	CS36042FB10	49.9K	CS34992FB10
R3	PR31	309K	CS43092FB16	270K	CS42702FB10	249K	CS42492FB18
R4	PR37	88.7K	CS38872FB18	93.1K	CS39312FB15	140K	CS41402FB14

	Madison,Park	M92,M96
PR91	25.5K/F_4 (CS32552FB11)	39.2K/F_4 (CS33922FB15)
PR89	100K/F_4 (CS41002FB28)	100K/F_4 (CS41002FB28)

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	+VGPU_CORE(MAX8792)	1A

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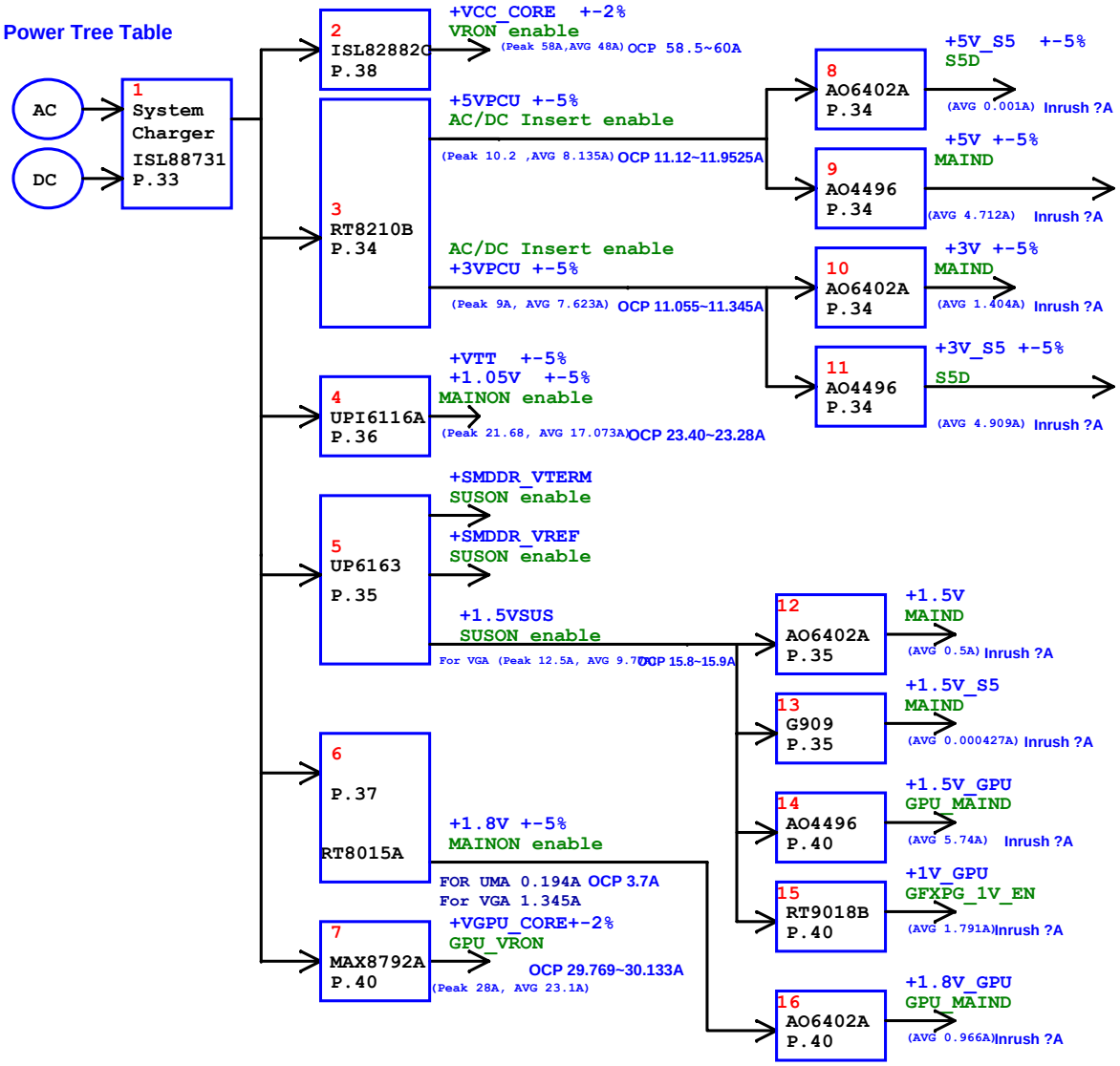
Power Tree Table



Power Distribution List

Power	Distribution

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2	Front Page	
3	Clock Generator	CLK
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9	RTC	RTC
15-16	DDRIII SO-DIMM	DDR
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18	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
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	TP&FP board	TPD,FPD
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	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
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28	FM Tunner	FMM
	Modem Connector	MDM
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29	Atheros LAN	LAN
30	NVRAM Connecyor	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

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PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

Model	REV	CHANGE LIST
TE2D MB	B2A	PAGE (16) : Add BT_EN# for combo RF control for BT PAGE (27) : Change DDR S3_1.5V ON circuit.
	C3A	PAGE (07) : Add ESATA re-driver IC
	D3A	PAGE(32) : LED luminance to light,R436、R427 1K-ohm change 2.2K-ohm. PAGE(32) : LED luminance too low,R428 560-ohm change 220-ohm. PAGE(27) : Add R230,R231,R286,R287 0.1-ohm to avoid speaker burn. PAGE(16) :Add Q62 to avoid leakage current.

MODEL TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
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14	1A	
15	1A	
16	1A	
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18	1A	
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23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

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PROJECT : TE2

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